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# LASER TRANSCEIVER ELECTRONICS I

J. S. Gray

Radiation, A Division of Harris-Intertype Corporation  
Melbourne, Florida

TECHNICAL REPORT AFAL-TR-73-282

July 1973



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## **LASER TRANSCEIVER ELECTRONICS I**

**J. S. Gray**

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## FOREWORD

This report was prepared by Radiation, A Division of Harris-Intertype Corporation, under Contract No. F33615-73-C-1026, Advanced Development Program 405B. This report covers the period 72 October 02 through 73 August 31, and is the final report on this contract. The work described herein was carried out by Radiation, A Division of Harris-Intertype Corporation, P.O. Box 37, Melbourne, Florida 32901.

The report was submitted in August 1973 and has been reviewed and is approved for publication.



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## ABSTRACT

A Laser Transceiver Electronics system was developed for use in an Air Force Program 405B brassboard 1 Gb/s laser communication system using quadrature phase shift key modulation on a single-frequency laser. This system contains a data source system, BER measurement system, 1 Gb/s QPSK modulator plus 100 kb/s PSK modulator, 1 Gb/s QPSK demodulator plus 100 kb/s PSK downconverter, and two each 500 Mb/s bit synchronizer-signal conditioners (BSSC). Synchronous combined modem-BSSC performance at 1 Gb/s is within 1.3 dB of the non-bandlimited PSK theoretical curve for BER's to  $10^{-6}$  over an automatic gain control range of 20 dB and with the 100 kb/s telemetry present. Nonsynchronous performance for close bit rates is within 0.2 dB of the synchronous curve.  $E_b/N_0$  on the downconverted telemetry IF output ranges from 20 to 30 dB for a wideband  $E_b/N_0$  range of 2 to 14 dB at the demodulator input. The conclusion is that 1 Gb/s QPSK signal processing has advanced to a state where operational hardware is practical.

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## Section I

### INTRODUCTION AND SUMMARY

During the Fall of 1972, Radiation started constructing a 1 Gb/s Laser Transceiver Electronics system for the Air Force Avionics Laboratory on Contract Number F33615-73-C-1026. This system contains a data source unit, bit error rate (BER) measurement unit, 1 Gb/s QPSK modulator plus 100 kb/s PSK modulator, 1 Gb/s QPSK demodulator plus 100 kb/s PSK downconverter, and two each 500 Mb/s bit synchronizer-signal conditioners. This equipment was shipped to LMSC, Palo Alto, by April 1, 1973 as scheduled, for integration in a Laser Communication System using quadrature phase shift-key modulation of a single-frequency laser. The Laser Transceiver Electronics system represents mature processing hardware that has excellent performance plus desirable operational system features. Synchronous 1 Gb/s system performance at  $10^{-6}$  BER is within 1.3 dB of the nonbandlimited QPSK theoretical curve over an AGC range of approximately 20 dB and with the 100 kb/s telemetry signal present. This hardware establishes the 1 Gb/s signal processing system as an operational prototype. A brief overview of the deliverable system is now presented in the next section.

## Section II

### SYSTEM OVERVIEW

#### 1. PERFORMANCE EVALUATION HARDWARE

A photograph of the performance evaluation hardware is given in Figure 1. The top unit is a link simulator that allows one to add baseband noise for performance testing of the BSSC or bandpass noise for testing of combined modem-BSSC performance. Filters are also provided for noise power measurements and for bandlimiting if desired. The SNR can be varied over a 9 dB range while S + N can be varied over a 20 dB range. Part of this unit was procured on a separate contract from the Laser Transceiver Electronics I contract.

The middle unit is a data source system that generates two independent uncorrelated 500 Mb/s data patterns of length  $(2^n - 2)$ . The data outputs can be selected to be synchronous or asynchronous. In the asynchronous mode, one bit rate is adjustable over a  $\pm 1\%$  range. There is also a 100 kb/s telemetry channel data output. The length of this sequence is  $(2^5 - 1)$ . The telemetry pattern simulates low-rate housekeeping data that would be transmitted along with the wideband information in an operational system.

The bottom unit is a BER (bit error rate) measurement system. After demodulation and processing in the BSSC's, the reconstructed wideband data outputs of both BSSC's are compared to the original data sequences and errors counted. Bit errors and bit errors divided by five are outputs on each 500 Mb/s channel. If BE/5 is counted, then the counter reading times  $10^{-8}$  is BER.

#### 2. 1 Gb/s QPSK MODULATOR PLUS 100 kb/s PSK MODULATOR

A simplified block diagram and photograph of this unit are presented in Figure 2. The two 500 Mb/s data inputs biphasically modulate two quadrature components of a 1.5 GHz stable frequency source. The biphasic modulator outputs are summed to generate a 1 Gb/s QPSK 1.5 GHz microwave subcarrier. This technique of generating QPSK as opposed to the series modulator approach allows the data inputs to be synchronous or asynchronous.

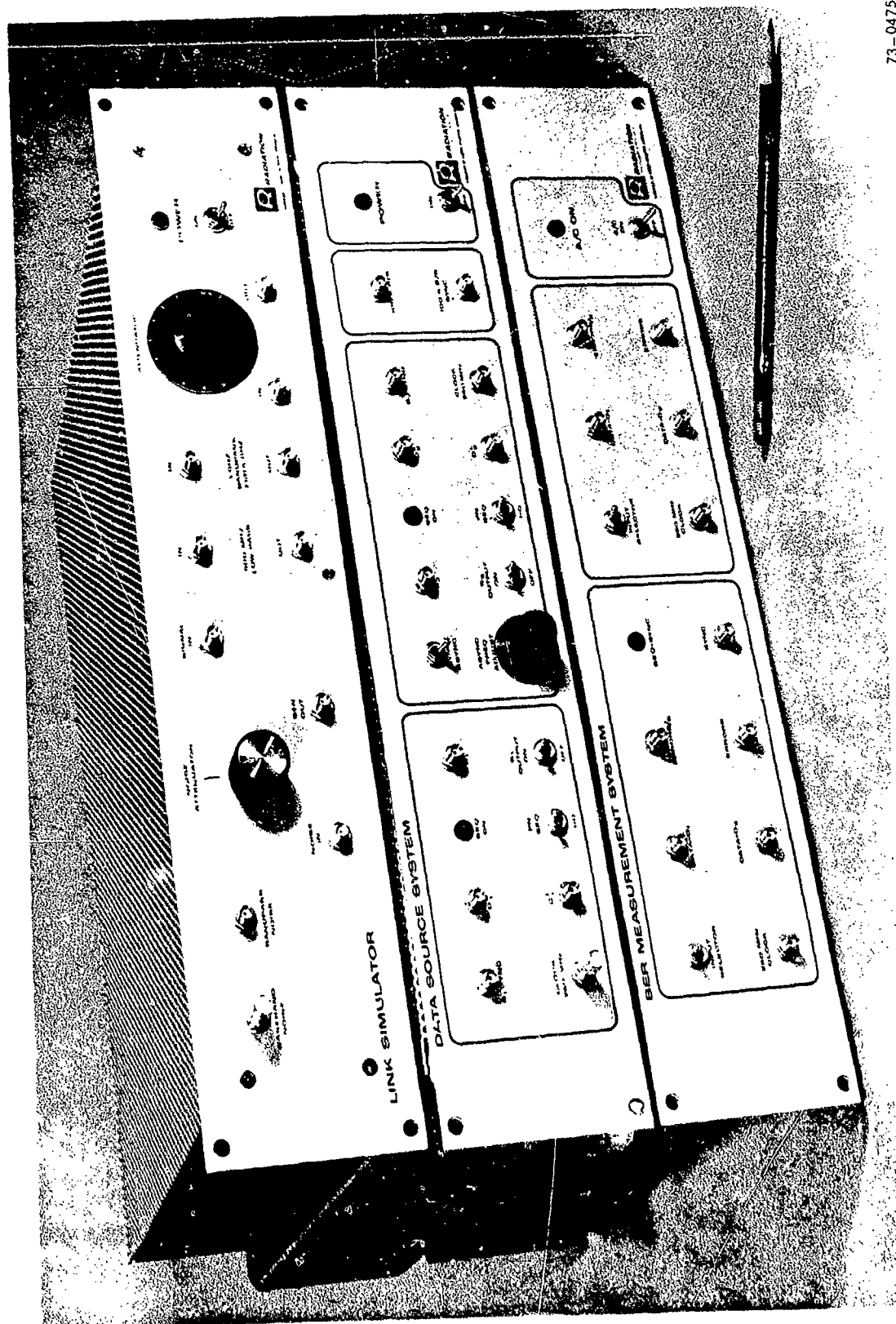
The 100 kb/s telemetry data input biphasically modulates a 1.03 GHz stable frequency source. The biphasic modulator output is attenuated and summed with the wideband modulated signal to generate the composite modulated signal. The amplified composite modulated signal is the overall output at a level of +5 dBm into a 50 $\Omega$  load. The ratio of wideband signal power to narrow band signal power is approximately 26 dB. It should be noted that the narrow band modulated subcarrier is placed in a null region of the wideband spectrum.

#### 3. 1 Gb/s QPSK DEMODULATOR PLUS 100 kb/s PSK DOWNCONVERTER

In Figure 3, a block diagram and photograph of the 1 Gb/s QPSK demodulator plus 100 kb/s PSK downconverter are presented. The composite modulated input plus noise is the input at a signal power level of -17 dBm to -37 dBm. The input is bandpass filtered by 2 GHz-wide filtering to eliminate out-of-band components and then amplified to provide the four outputs, X(t). The amplification is automatic gain controlled such that X(t) is essentially constant for a 20 dB variation of the input. Two of the X(t)'s are mixed with quadrature components of a 1.5 GHz coherent reference to provide the demodulated 500 Mb/s output data streams.

Another X(t) is bandpass filtered, amplified, and routed through an X4 multiplier to produce a 6 GHz unmodulated reference. In the phase-lock loop a 6 GHz X4 output of a 1.5 GHz VCO is phase locked to the 6 GHz reference input. The 1.5 GHz VCO then provides the coherent reference for demodulation. This coherent reference is adjusted in phase, power divided into quadrature components, fine phase adjusted, and routed to the data detectors.

The bottom X(t) is narrow band filtered and mixed with a 1 GHz stable reference to downconvert the biphasic PSK 1.03 GHz telemetry signal to a 30 MHz IF frequency. The 100 kb/s PSK 30 MHz signal is filtered, amplified by approximately 70 dB, and then provided as an output.



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Figure 1. Performance Evaluation Hardware

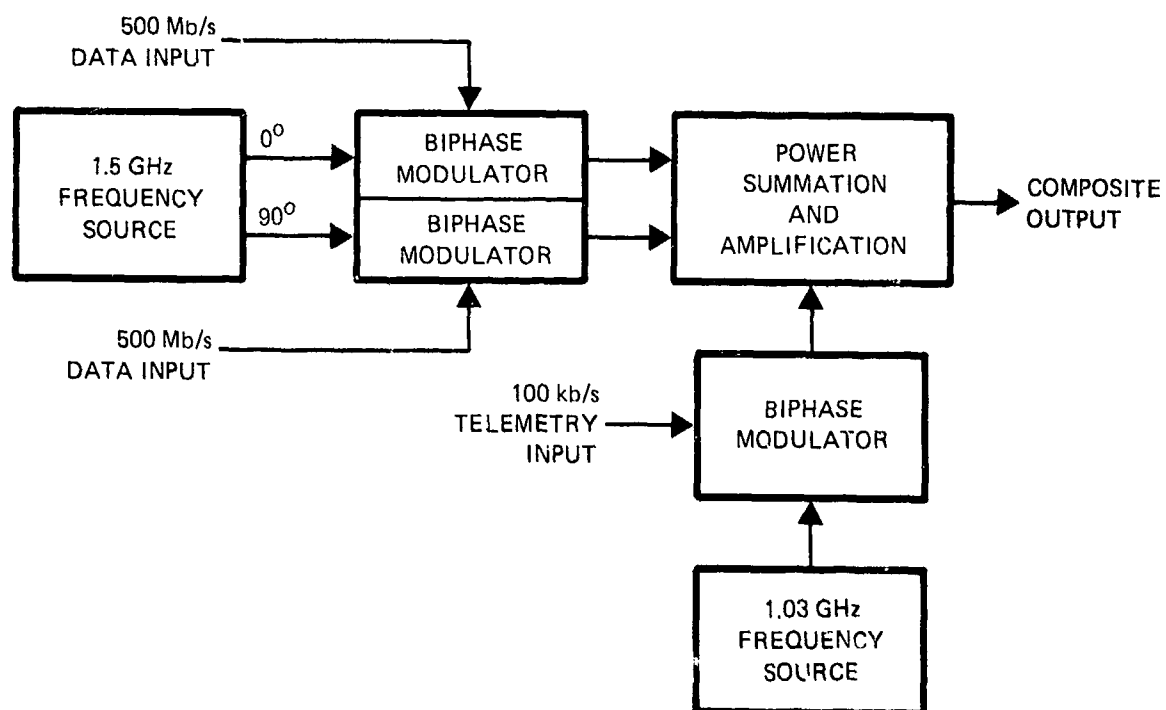
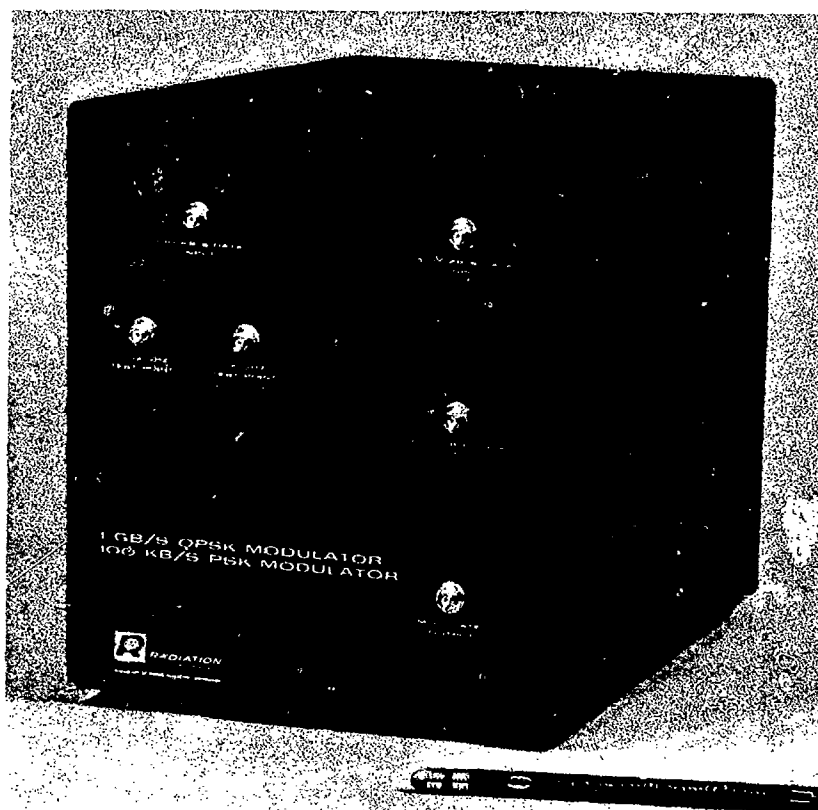


Figure 2. 1 Gb/s QPSK Modulator Plus 100 kb/s PSK Modulator

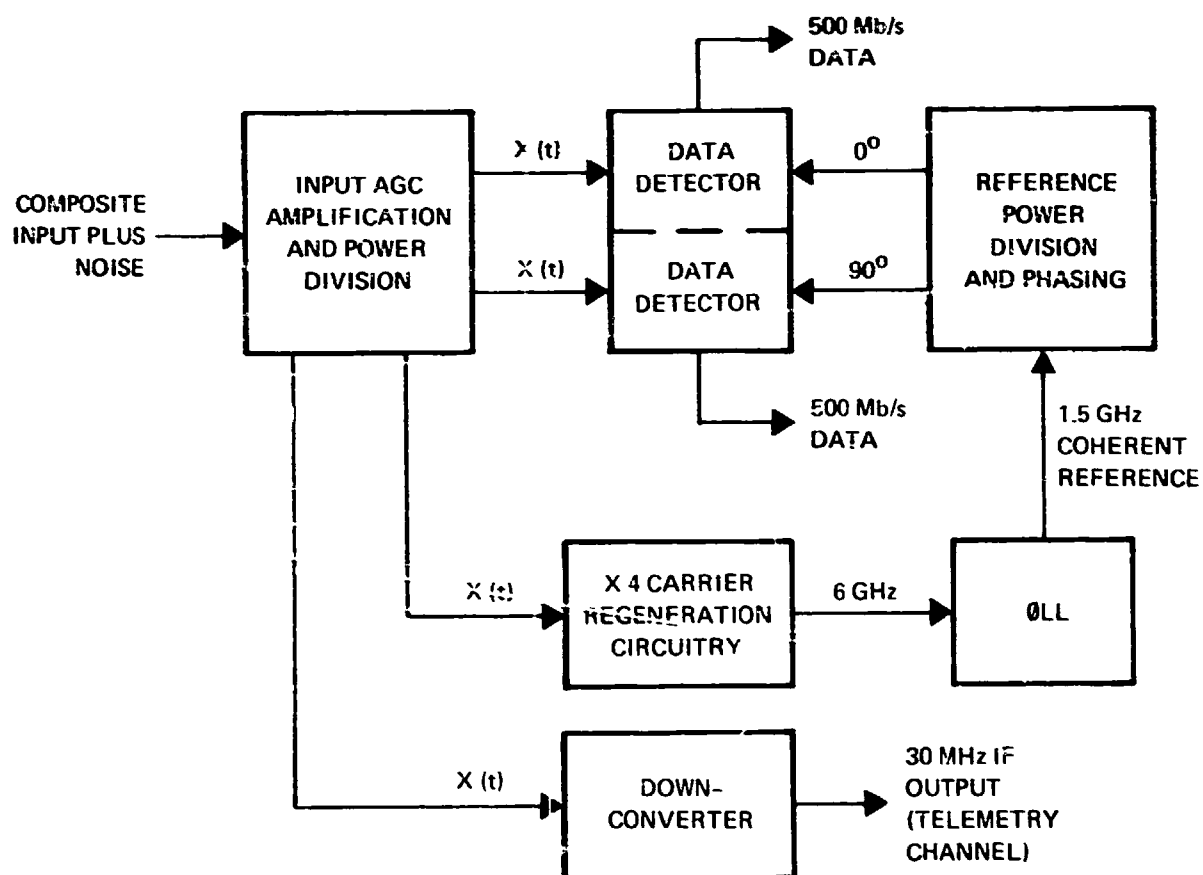
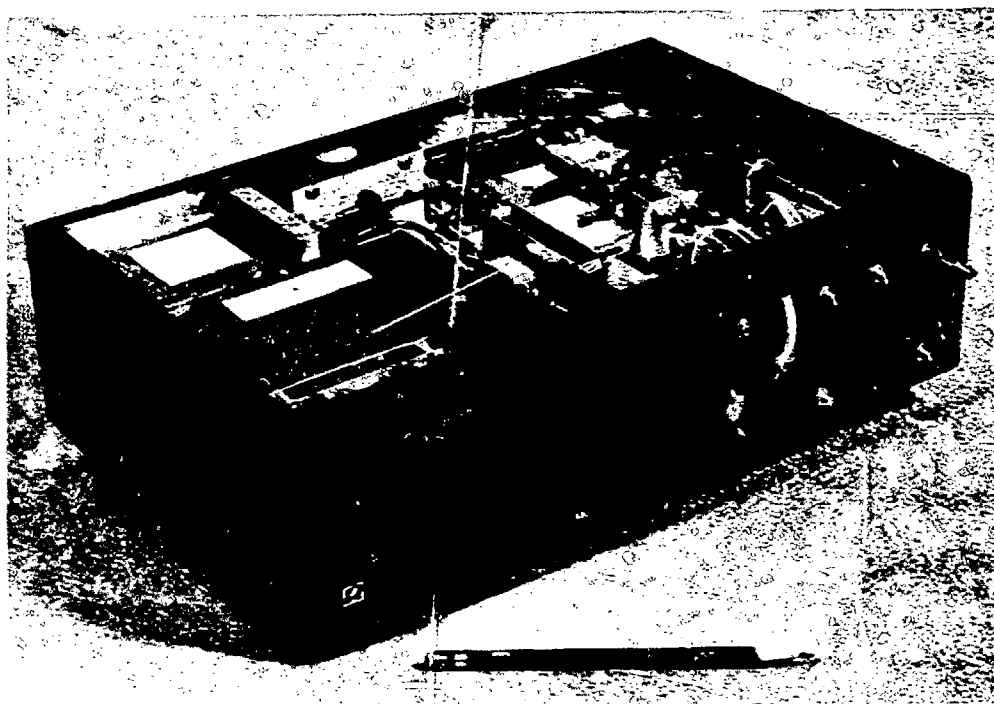


Figure 3. 1 Gb/s QPSK Demodulator Plus 100 kb/s PSK Downconverter

#### 4. 500 Mb/s BIT SYNCHRONIZER-SIGNAL CONDITIONER (BSSC)

A photograph and block diagram of the 500 Mb/s bit synchronizer-signal conditioner (BSSC) is presented in Figure 4. The baseband PCM plus noise output of the demodulator is routed to the BSSC input. The  $S + N$  is processed and amplified in the matched filter to provide two isolated outputs,  $Y(t)$ . The time invariant filter is an approximation of the sliding integral matched filter but is adjustable. For baseband operation, the filter is adjusted to synthesize a matched filter. When operated with the QPSK demodulator, the filter is adjusted such that the combination of the analytic low-pass equivalent filtering of the demodulator and the BSSC filter represents a matched filter. The variability of the BSSC filter also allows compensation for the filtering of other system components.

In one path  $Y(t)$  is routed to a decision unit where  $Y(t)$  is compared to a reference level,  $\Sigma$ . A narrow pulse is generated if  $(Y(t) - \Sigma)$  is negative at the end of a given bit period. If  $(Y(t) - \Sigma) > 0$  at the end of the bit period, no pulse is generated. These pulses are the input to logic circuitry that generates a 500 Mb/s data estimate bit stream. The timing of the decision process is controlled by the bit rate clock output of the bit synchronizer. The 500 Mb/s data estimate output is also demultiplexed into two output 250 Mb/s data streams at MECL III levels for convenience in testing. The bit rate clock divided by two controls the demultiplexer and is also provided as an output.

In the other path  $Y(t)$  is nonlinearly processed to generate a bit rate spectral component. This component is bandpass filtered to improve SNR and to provide memory for periods of no transitions and then amplified to provide the reference for the phase-lock loop (PLL). The output of the 500 MHz VCO in the phase-lock loop is phase locked to the reference bit rate input. The VCO output is routed to the decision unit and demultiplexer and is also provided as an overall output.



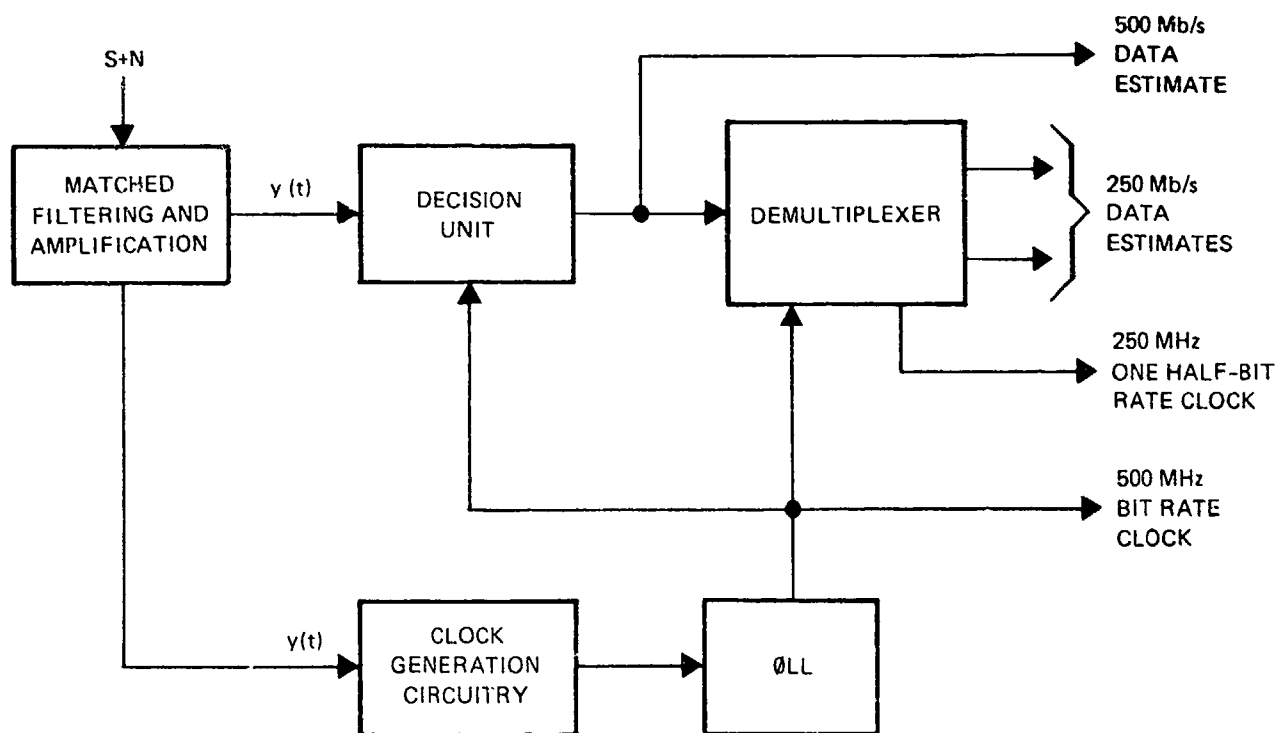
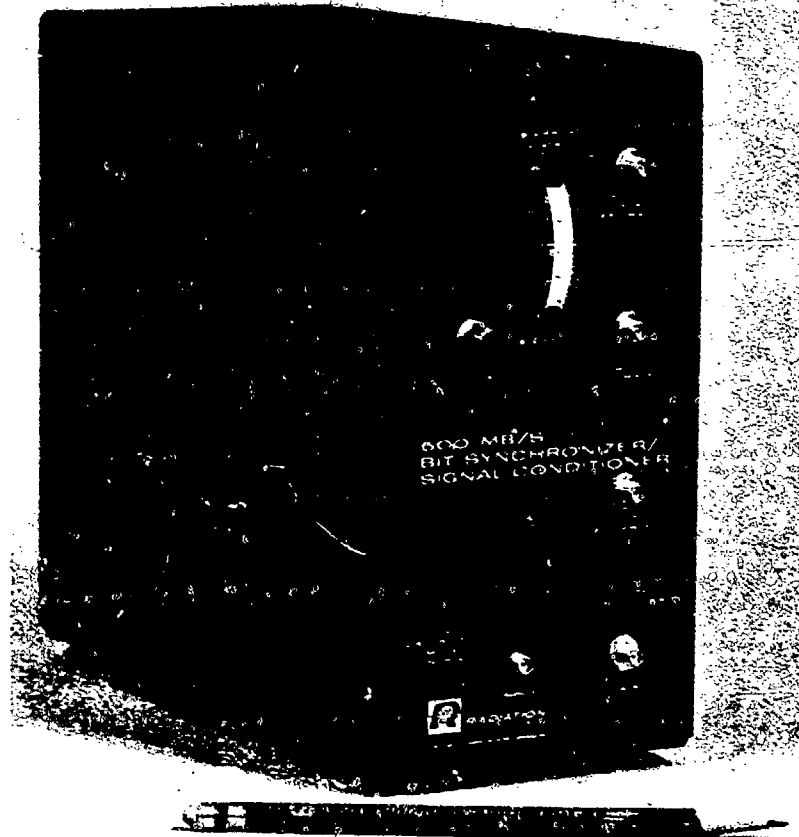


Figure 4. 500 Mb/s Bit Synchronizer-Signal Conditioner (BSSC)

### Section III

#### DESIGN CONSIDERATIONS FOR THE DATA SOURCE AND BER MEASUREMENT SYSTEM

A photograph of these units along with a link simulator unit is presented in Figure 5. The design approach for both systems is now presented.

##### 1. DATA SOURCE SYSTEM

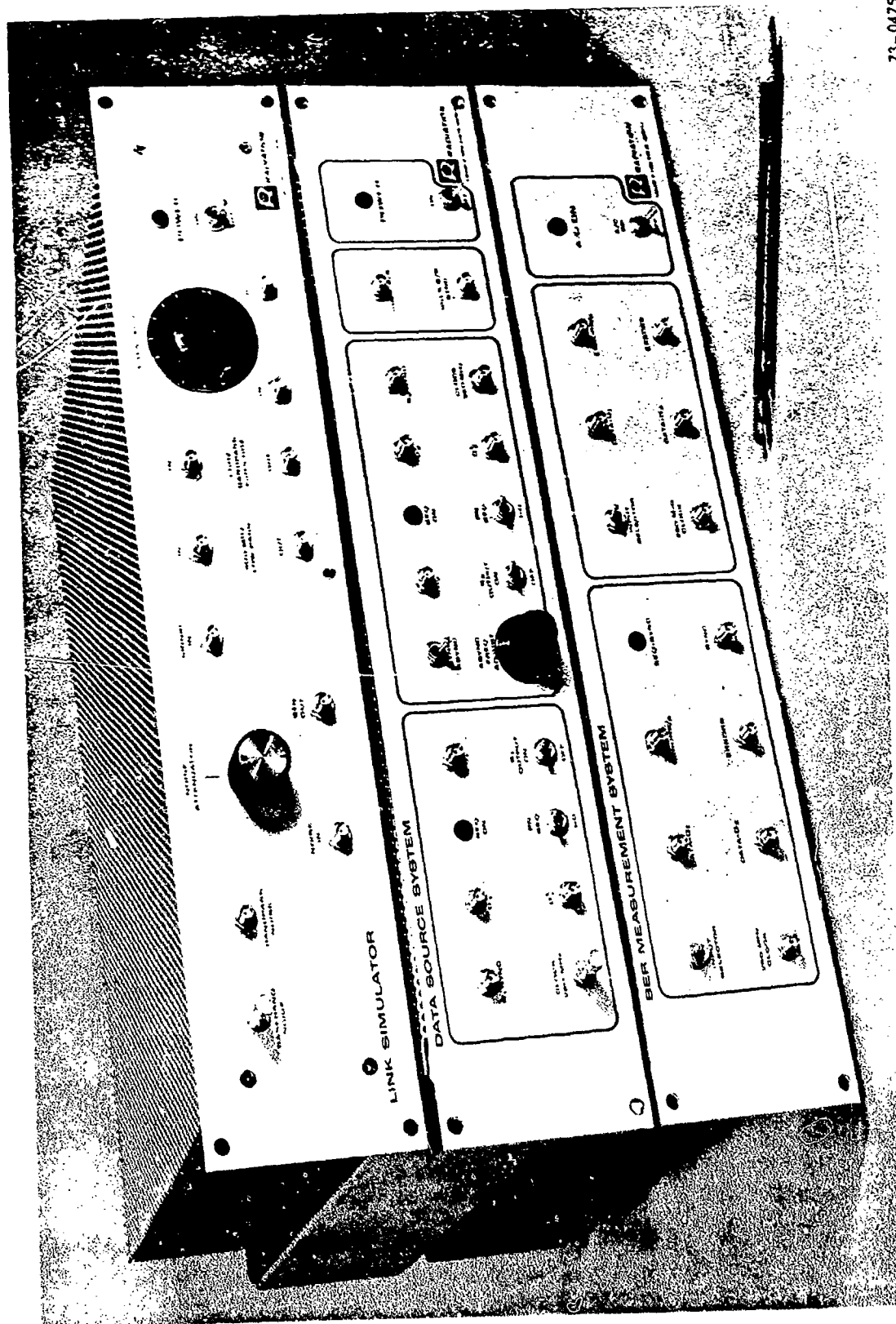
A block diagram of the data source system is given by Figure 6 and Figure 7. The basic technique consists of generating a PN sequence at 250 Mb/s and then multiplexing two taps separated by N bits to form the 500 Mb/s data stream. The basic reason for this approach is simply one of cost. A 250 MHz monolithic flip-flop costs approximately \$20 while a 500 MHz monolithic flip-flop costs approximately \$50 to \$60. Building discrete logic or logic with hybrid techniques in the 500 MHz to 1000 MHz region usually results in a flip-flop cost of approximately \$200. Therefore, it is much more cost-effective to use mainly 250 MHz logic and then multiplex to generate the 500 Mb/s data stream. Likewise, demultiplexing at the input to the BER measurement system allows the use of the lower cost 250 MHz logic in its circuitry.

As shown in Figure 6 there are two data generators. The PN sequence in both is of length  $(2^{10} - 1)$  but different generating polynomials are used so that the sequences are uncorrelated. The same delay of N bits between each sequence and its delayed replica input to the multiplexer is used to simplify the BER measurement technique as explained later. N is chosen as 14 bits to eliminate any correlation between signal processing decisions made by the communications system on a given bit and its delayed replica in the multiplexed bit stream 2N or 28 bits later.

The method of implementation can be explained by reference to Figure 6. The 250 MHz crystal oscillator output is power split into two paths. In the upper path, this clock is further power split to drive the  $(2^{10} - 1)$  PRN sequence generator, the sync pulse correlator, and the multiplexer. The sequence generator creates a  $(2^{10} - 1)$  PRN sequence. Two shift register stage outputs separated by N bits are routed to the multiplexer where a  $(2^{11} - 2)$  length 500 Mb/s data stream is created. A shift register stage output of the sequence generator is also routed to the sync pulse correlator. This correlator detects the all "Ones" condition in the sequence and generates a frame sync pulse upon such detection. The frame sync pulse output allows one to externally synchronize an oscilloscope such that individual bits of the 500 Mb/s data stream may be displayed. The digital output of the multiplexer is transformed in the output converter to a bipolar NRZ data stream with fast rise and fall times.

In the lower half of the figure there is a block diagram of similar circuitry which generates a second but independent (no correlation) 500 Mb/s data stream by generating a different 250 Mb/s length  $(2^{10} - 1)$  PRN sequence. There is also a switch at the clock input to allow one to choose the internal 250 MHz clock for synchronous operation or a separate variable rate clock for asynchronous operation. The specification for the variable source frequency and its variation is 250 MHz  $\pm 1\%$ . This generates a 500 Mb/s  $\pm 1\%$  output. Since separate 500 Mb/s data sources in an operational system would probably be controlled by crystal oscillators, it is hard to conceive how frequency differences could ever exceed 1 percent. The only exception to this would be an operational situation where the asynchronous data sources were deliberately very different in bit rate; for example, 500 Mb/s and 200 Mb/s. For this case, the modem hardware would remain the same but the BSSC on the 200 Mb/s channel would differ.

The variable rate frequency source poses several problems. A 250 MHz crystal oscillator mechanically tuned or crystal VCO does not have enough tuning range. A 250 MHz LC oscillator mechanically tuned or an LC VCO has the range but not enough stability. The variable frequency source technique which overcomes these difficulties, is shown in Figure 7. A 25 MHz LC type VCO with a center frequency of 25 MHz and  $\pm 5\%$  tuning range is mixed with a 225 MHz crystal oscillator output. The sum frequency is 250 MHz  $\pm 1\%$  and is selected by a bandpass filter centered on 250 MHz. The filter output is then amplified to provide the proper drive levels for data source #2 when variable rate clock is selected.



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Figure 5. Performance Evaluation Hardware

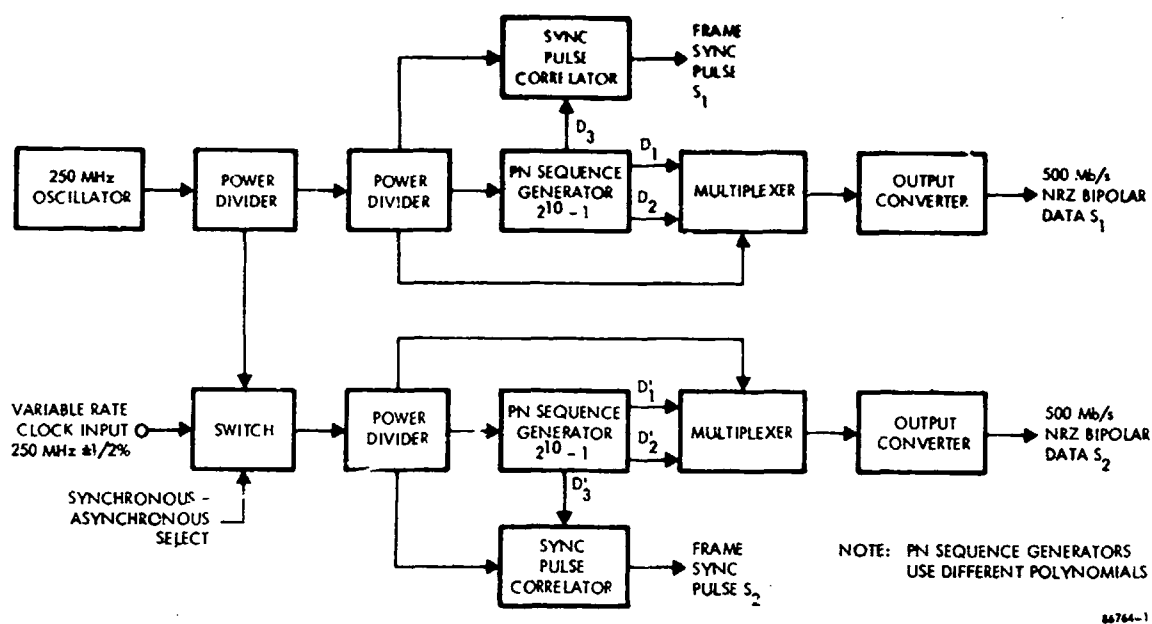


Figure 6. Data Source System - Data Generator

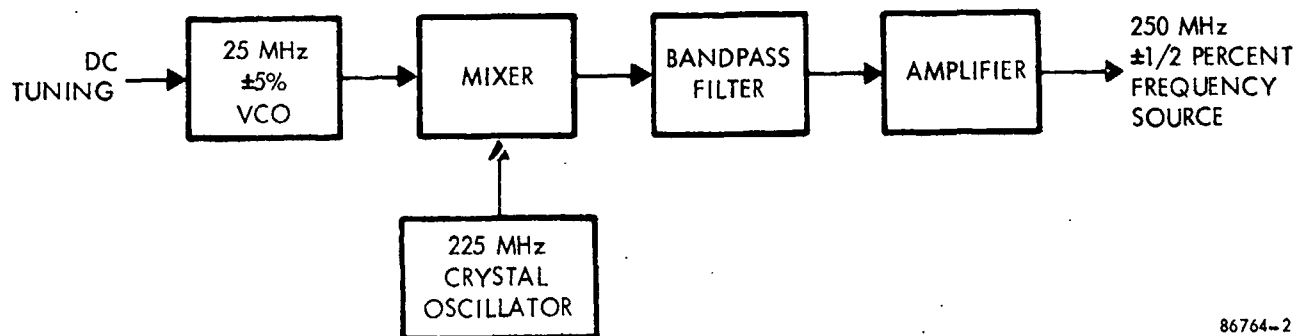
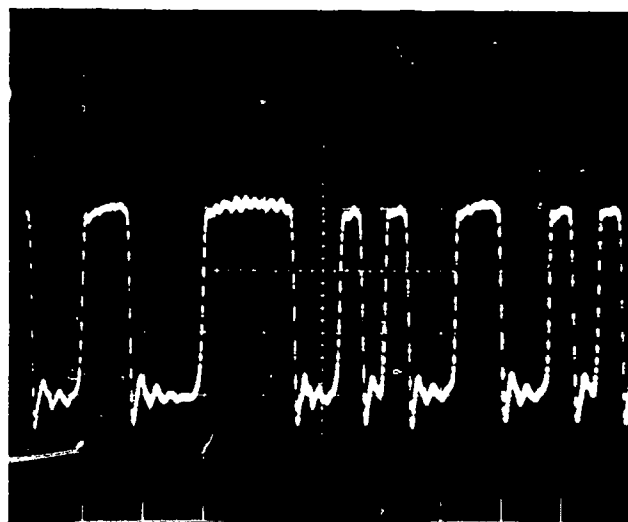


Figure 7. Data Source System - Variable Rate Frequency Source

A picture of several bits of the signal output of the data source system in the time domain is provided in Figure 8. Rise and fall times are approximately 350 picoseconds. A picture of the  $(\sin x/x)^2$  spectrum from 0 to 2 GHz is shown in Figure 9. There is significant response out to four times the 500 Mb/s bit rate and bandlimiting is not perceivable until the third lobe of the spectrum.

## 2. BIT ERROR RATE (BER) MEASUREMENT SYSTEM

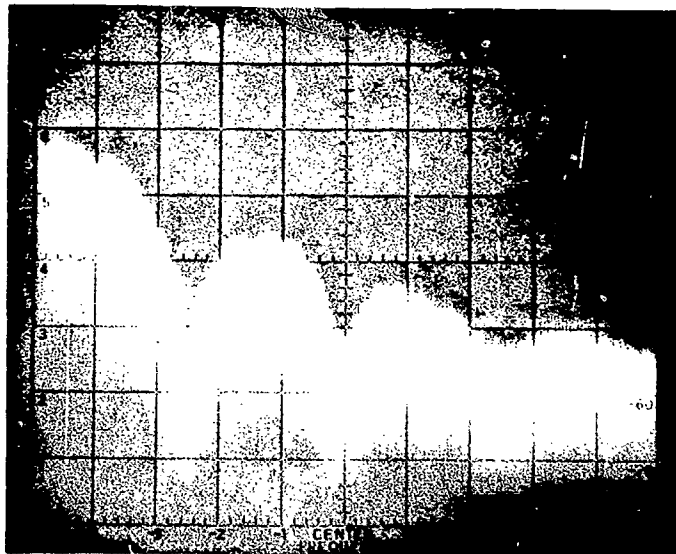
The technique used in the BER measurement unit is based upon the fact that each of the two 500 Mb/s data source bit streams is composed of a multiplexed early and delayed version of a 250 Mb/s PRN sequence. In each BSSC, an estimate of one of the two 500 Mb/s data streams is demultiplexed into estimates of the two original data sequences. The selected technique consists of delaying the early PRN sequence estimate by  $N$  bits and comparing it in an error detector against the late PRN sequence estimate.  $N$  is chosen to be 14 bits, the original delay between the two sequences, such that the delayed early PRN sequence lines up timewise with the late PRN sequence at the input of the error detector. Therefore, if there is no error in either sequence estimate, then the error output



50 mV/DIV  
5 nSEC/DIV

86764-15

Figure 8. Time Domain Output of Data Source System



VERTICAL  
10 dB/DIV

HORIZONTAL  
0 - 2.0 GHz  
200 MHz/DIV

86764-16

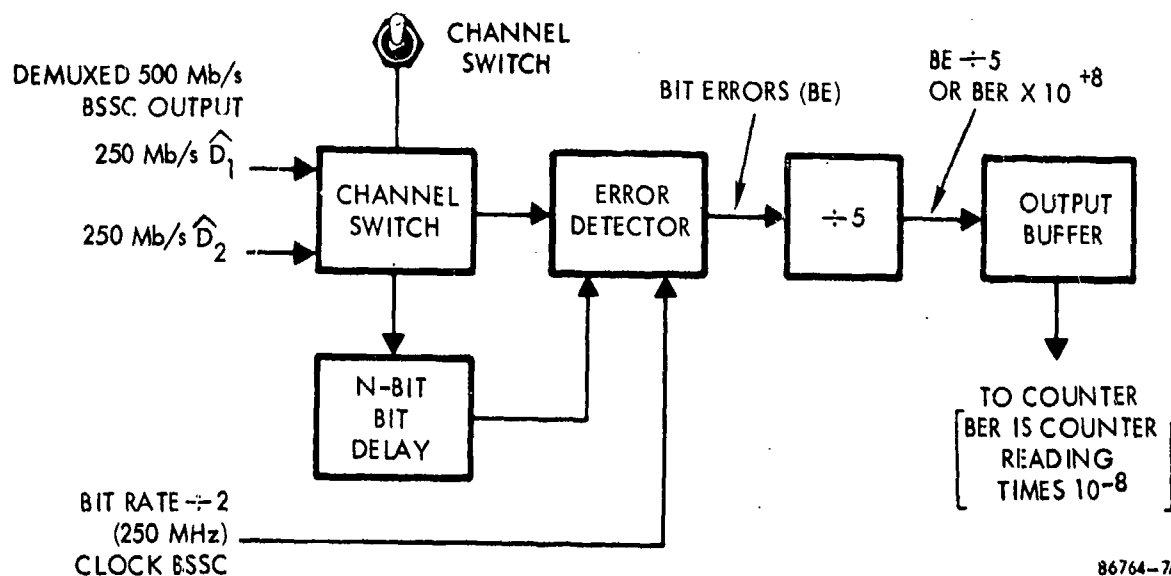
Figure 9. Frequency Domain Output of Data Source System

of the error detector is zero. Any error in either estimated bit stream produces an error count except for the case where, during a given bit time, an error is simultaneously made in both data estimates. For an  $N$  bit delay between the two 250 Mb/s data streams there is a  $2N$  bit delay between corresponding bits in the 500 Mb/s data stream.  $N$  was chosen as 14 bits so that the decision process in the BSSC can be considered completely independent for bits  $2N$  or 28 bits apart. With independent decisions it is simple to calculate the percentage error in the overall bit error rate sample mean due to simultaneous errors in both data estimate data streams. This is presented in Table 1. It is seen that the error in the measured error rate is less than 1 percent for error rates as large as  $10^{-2}$ . A 1-percent difference is indiscernible on a BER versus SNR curve. In fact, even a 100-percent difference represents less than several tenths of a dB difference at any given reasonable SNR, and measurement accuracy on a high bit rate system is probably no better than  $\pm 1/2$  dB. At the error rates of prime interest, i.e.,  $< 10^{-3}$ , the error is much less than 0.1 percent.

Table 1. Effect of Simultaneous Errors in Comparing Two Data Estimate Bit Streams

Actual Bit Error Rate	Error in Percent in Measured BER Due to Simultaneous Errors
$10^{-9}$	$-10^{-7}\%$
$10^{-7}$	$-10^{-5}\%$
$10^{-5}$	$-0.001\%$
$10^{-3}$	$-0.1\%$
$10^{-2}$	$-1\%$

Such a technique is simple and has several operational advantages. A simplified block diagram of the BER measurement part of the overall test system is presented in Figure 10. The two 250 Mb/s data estimate outputs of



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Figure 10. BER Measurement System -- Simplified Block Diagram

the BSSC are connected to the channel switch. The logic is controlled by a front panel switch so that the outputs can be interchanged. The switch is set such that the early 250 Mb/s PRN sequence is routed through the N bit delay to the error detector so that both sequences are shifted into the error detector in alignment. These are compared against each other bit by bit, and differences or errors are counted. The bit errors are divided by five and converted to a signal suitable for driving a counter. The overall output is (bit errors  $\div$  5) or BER  $\times 10^8$ .

What are the advantages of such a system? First, two separate independent 500 Mb/s data sources were used. Each was comprised of two PRN sequences separated by N bits multiplexed together. As long as the delay N between multiplexed sequences is the same, the test system can handle either data source even though they are totally uncorrelated and comprised of different sequences. Second, an inversion in demodulation causes both demultiplexed data streams to be inverted so that operation of the error detection circuitry is the same. Thus, all the QPSK demodulation variations are automatically handled because the measurement system is transparent to whether it receives demultiplexed data from  $S_1$ ,  $S_2$ ,  $-S_1$  or  $-S_2$ . Third, synchronization is not required. The only control required is the channel switch which handles the ambiguity in BSSC demultiplexing. If the BSSC outputs are routed improperly, the BER is 25 percent. One merely observes this condition and throws the channel switch to the opposite position and operation is immediately that desired without synchronization. In summary, it is seen that the eight possible selections due to separate 500 Mb/s data sources, QPSK demodulation ambiguity, and BSSC demultiplexer ambiguity are reduced to two selections controlled by a simple switch and that there is no synchronization requirement.

The detailed BER measurement system block diagram is presented in Figure 11. It is seen that it basically consists of two units like the one shown in the previous block diagram from test number 2. Thus, BER measurements can be made simultaneously on both 500 Mb/s BSSC data estimate outputs. One item shown in this block diagram that was not discussed in the previous block diagram is the clock phasing circuitry. When the demultiplexed outputs from the BSSC are interchanged to properly compare bit streams for BER measurements, it can be shown that the one-half bit rate clock from the BSSC should be adjusted in phase by 180 degrees so that the data streams are shifted into the error detector input flip-flops correctly. This is accomplished by dc biphase modulating the one-half bit rate clock according to the interchange switch position.

The ability to handle independent data sources and to reduce an eight-state ambiguity problem to a simple two-state switch setting with automatic synchronization is considered quite significant. The author has tested QPSK system for several years and feels that the ease of testing with this system is probably not fully appreciated unless one has had to test such systems using different techniques. If desired, the system could be fully automated in the following manner. The bit errors/5 output could be counted by internal circuitry. If the count per unit time exceeded a maximum number for error rates to be expected in normal usage, then logic would cause the BSSC outputs to be interchanged and the one-half bit rate clock phase to change by 180 degrees. Thus, even the two-state front panel switch would be eliminated.



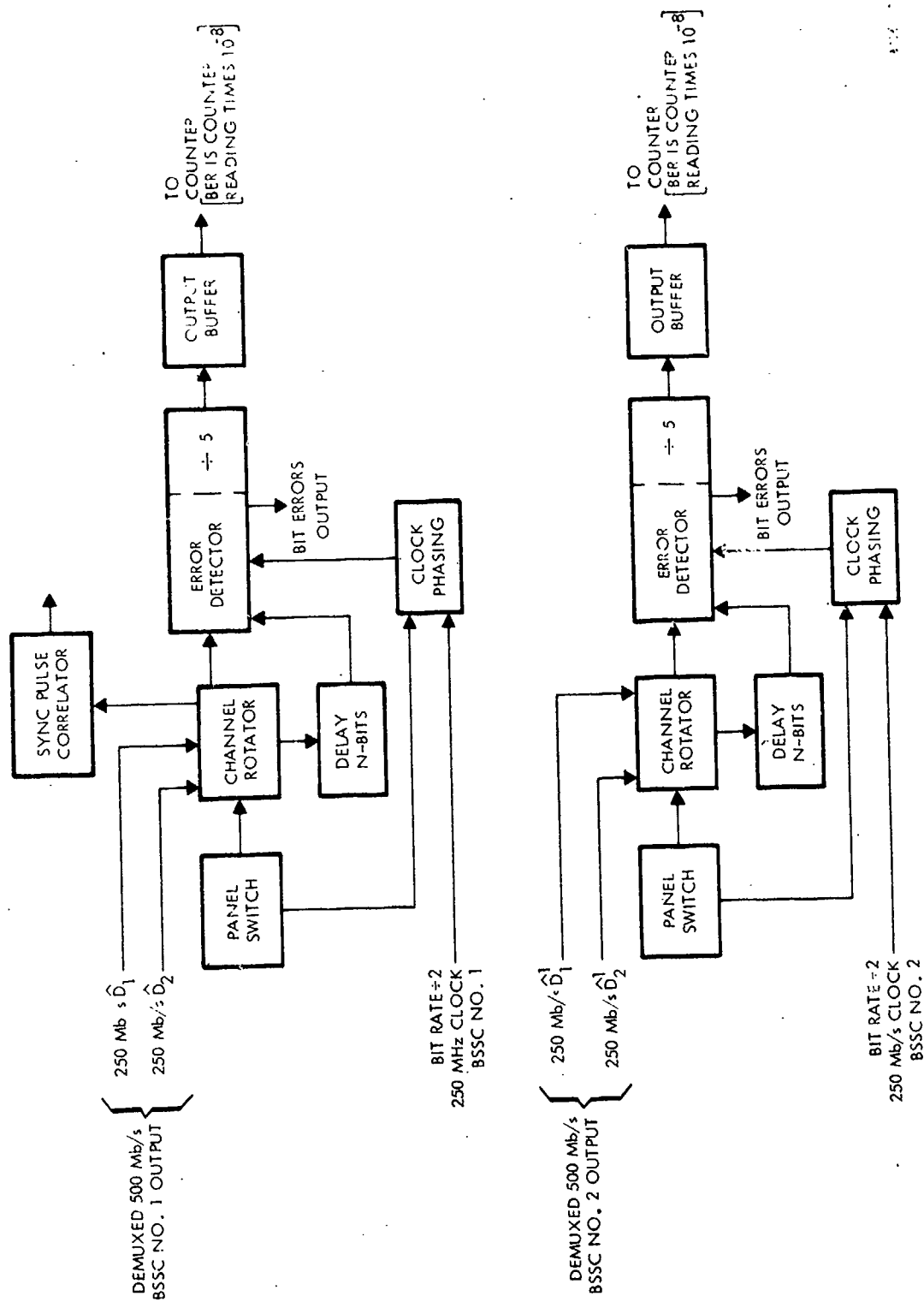


Figure 11. BER Measurement System - Detailed Block Diagram

## Section IV

### DESIGN CONSIDERATIONS FOR MICROWAVE MODULATOR AND DEMODULATOR

#### 1. 1 Gb/s QPSK MODULATOR PLUS 100 kb/s PSK MODULATOR

A photograph and simplified block diagram of this unit are repeated in Figure 12. This unit contains both a wideband 1 Gb/s QPSK modulator and a narrow band 100 kb/s PSK modulator. Since the ratio of the wideband signal power to narrow band signal power is 26 dB, the narrow band spectrum is easily summed with the wideband spectrum in a resistive power summer with adequate padding on the narrow band port of the power splitter to prevent degradation of the VSWR of the wideband signal connections. Various modem functions were subjected to detailed testing on this program during the first couple of months. Experience had been previously gained on discrete amplifiers having a .5 to 2.5 GHz bandwidth that was a special design by the vendor. The same vendor had later supplied measured S parameters over the same frequency range (.5 to 2.5 GHz) for his 1 to 2 GHz thin-film amplifier modules. The computer was used to convert the data into voltage gain in terms of magnitude and phase, input VSWR, and output VSWR for a cascade of the thin-film modules having overall equivalent gain specifications equal to the discrete amplifiers. This was done for multiple units since data was supplied for several units of each type. The results of this investigation showed that the thin-film unit could be used over a 2 GHz bandwidth and had performance equal to or exceeding the discrete amplifiers. Therefore, it was decided to use the thin-film amplifiers in the deliverable modem hardware. As a further test the thin-film amplifiers ordered on the Laser Transceiver Electronics program were tested over the same 2 GHz bandwidth on an HP network analyzer. The results were consistent with the earlier tests. The measured performance on one of the amplifiers is presented in Figure 13 and Figure 14. Since these amplifiers occupy less than 1/6 of the volume of the discrete amplifiers and consume equal or less power, they allow a reduction in overall modem size to anticipate the design of satellite hardware.

Extensive mixer tests were used to select the mixers for the system. The tests included such things as mixer conversion loss as a function of frequency, conversion loss as a function of biphase state, in-band baseband feedthrough, out-of-band baseband feedthrough, and finally performance in a hard wired timed biphase modulator-demodulator test fixture. "Real-world" mixers do not behave at all like the nice product functions we describe them as in textbooks. For example, as biphase modulators they usually don't switch the carrier phase by 180 degrees and the amount of phase shift through the mixer is a function of the carrier frequency. The conversion loss also varies with frequency. Finally, part of the baseband drive energy appears in the bandpass spectrum of interest. With biphase systems some of the above deficiencies degrade performance slowly and gracefully. In quadrature PSK systems their effect is more pronounced since the four-phase states are generated by adding complex vectors. A requirement for good performance in QPSK systems is proper matching of mixer pairs. Mixers are, in general, not sold to any sort of matching criteria so one must test a sample lot to select suitable pairs. With the growth of QPSK systems vendors are now seriously considering the matching problem. By using the tests described previously pairs of mixers were chosen for the deliverable modem. The tests indicated that different mixers should be in the QPSK modulator and the QPSK demodulator. It was experimentally verified that this optimized overall combined modem-BSSC performance as predicted. Therefore, such mixer pairs were used in the deliverable system.

After statistical subsystem testing proved that various functional blocks were truly optimum, they were used in the deliverable system. This statement about system testing being the final test for all functions should be amplified. If one tests a function that has been implemented using a new technique and finds that the performance of the function alone is superior in multiple ways to its predecessor, then it is reasonable to expect system statistical performance to be better or, at least, not degraded. In general, this has happened experimentally. Often, however, one improves one characteristic of the device but degrades slightly another characteristic. For example, the magnitude of the frequency response is flatter over a greater frequency range but the phase becomes more nonlinear at one extreme of the frequency range of interest. In such a case the final and conclusive test is the effect of the new function on overall system statistical performance. It should be noted that the nonideal characteristics of the various functions are often such that it is analytically very difficult to predict in such a case the effect of such a

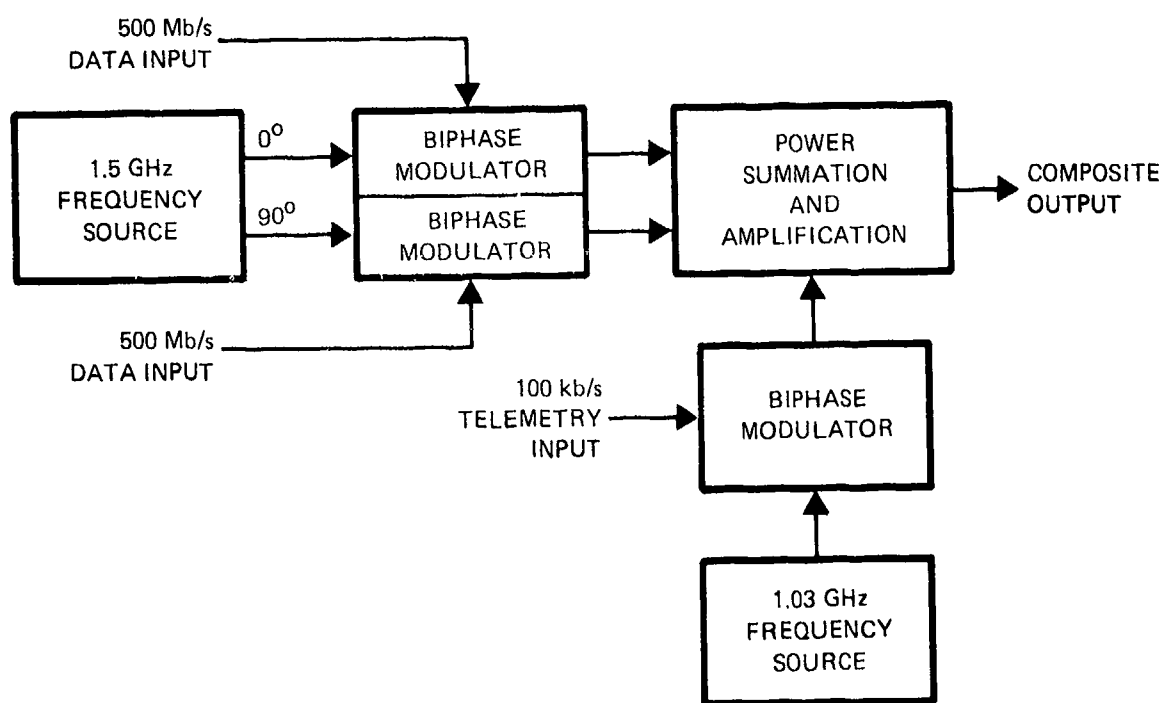
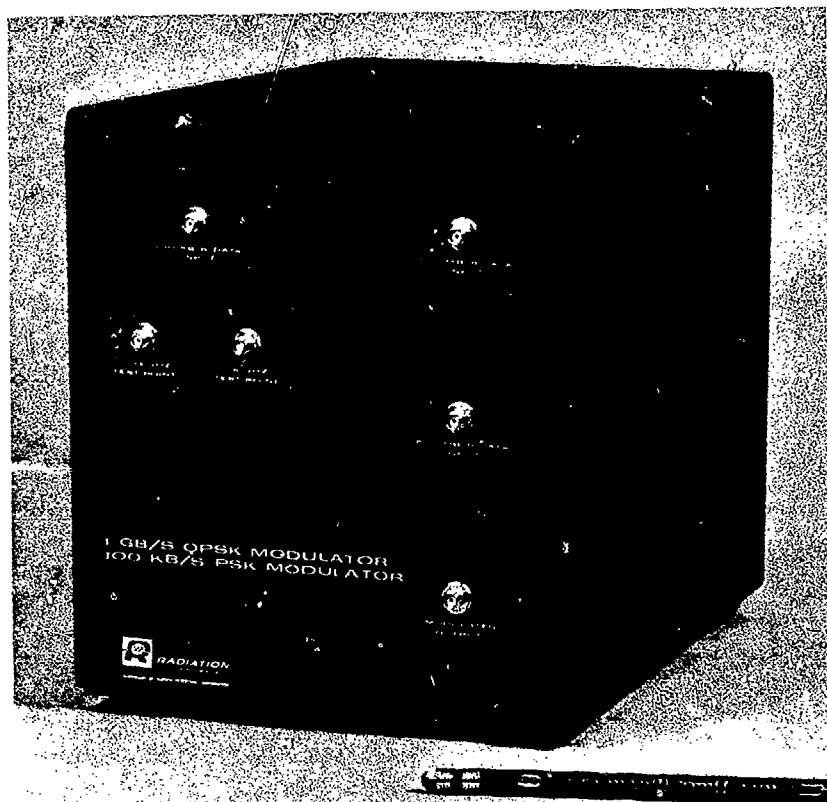


Figure 12. 1 Gb/s QPSK Modulator Plus 100 kb/s PSK Modulator

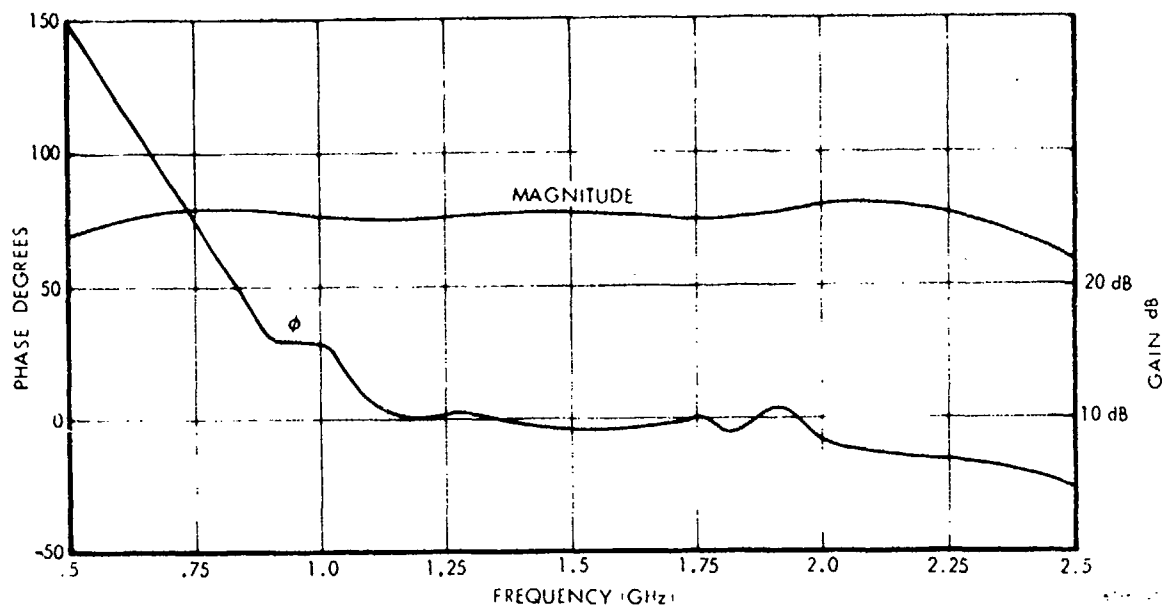


Figure 13. Frequency Response for Thin-Film Amplifier

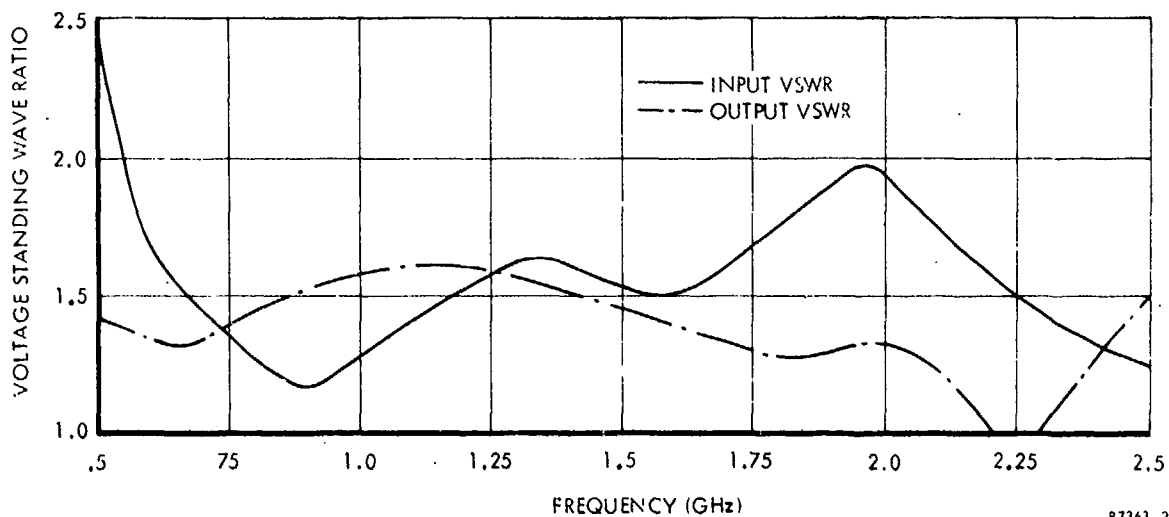


Figure 14. Input and Output VSWR for Thin-Film Amplifier

change. The previous does not intend to downgrade analysis. In fact, these systems have measured performance typically within 0.2 dB of that predicted analytically. It merely recognizes that the final detailed design of such systems involves some art as well as science.

## 2 1 Gb/s QPSK DEMODULATOR PLUS 100 kb/s PSK DOWNCONVERTER

A block diagram and photograph of this unit are repeated in Figure 15. As discussed in Chapter II, the composite signal input is automatic gain control amplified and power split into four identical signals,  $X(t)$ , in four separate paths. In the downconverter path the total signal passes through a 0.3 percent bandwidth filter centered at 1.03 GHz. The filter output is mixed with a 1 GHz crystal reference so that the telemetry signal centered at 1.03 GHz is translated to a difference frequency of 30 MHz. The mixer output is amplified by 70 dB in a 400 kHz wide IF amplifier centered at 30 MHz. In the delivered system the effect of the telemetry channel on wideband BER performance was negligible but at the same time the measured output SNR of the downconverter was very high so that extremely low error rate telemetry decisions could be made.

The AGC loop design was standard except that the desired 2 GHz bandwidth for the variable loss element was a problem. Only one vendor would bid on the unit and his range was specified at 15 dB instead of the desired 20 dB. Within the cost and time constraints of the contract, it was felt that it would be sagacious to use this device rather than attempt an in-house design. The requirements on the AGC loop were minimal. The bandwidth of the AGC loop was chosen at 200 Hz. This low value for bandwidth is well below the phase-lock loop bandwidth, yet allows a reasonable response to input power fluctuations due to laser power supply effects. The gain of the loop was specified such that the power out of the AGC amplifier will not change more than .5 dB over the input range of approximately 20 dB. Such a small change in output power will cause minimal degradation in the performance of the bit synchronizer and, likewise, will not degrade the performance of the carrier regeneration phase-lock loop. Thus, we specify that:

$$BW = 200 \text{ Hz}$$

$$\Delta \text{ att} = .5 \text{ dB}$$

The loop can be analyzed utilizing an equivalent linear model provided that the transfer function of the AGC network is linear in decibels per volt. This transfer function was measured. Utilizing the results of this measurement, a reasonably linear approximation of the transfer function can be expressed as follows:

$$K_A = 1.75 \text{ dB/volt}$$

Another constant that will be used in the loop analysis is the transfer function of the detector. This constant can be expressed as:

$$K_d = .15 \text{ volt, dB}$$

The loop can now be analyzed utilizing the following model.

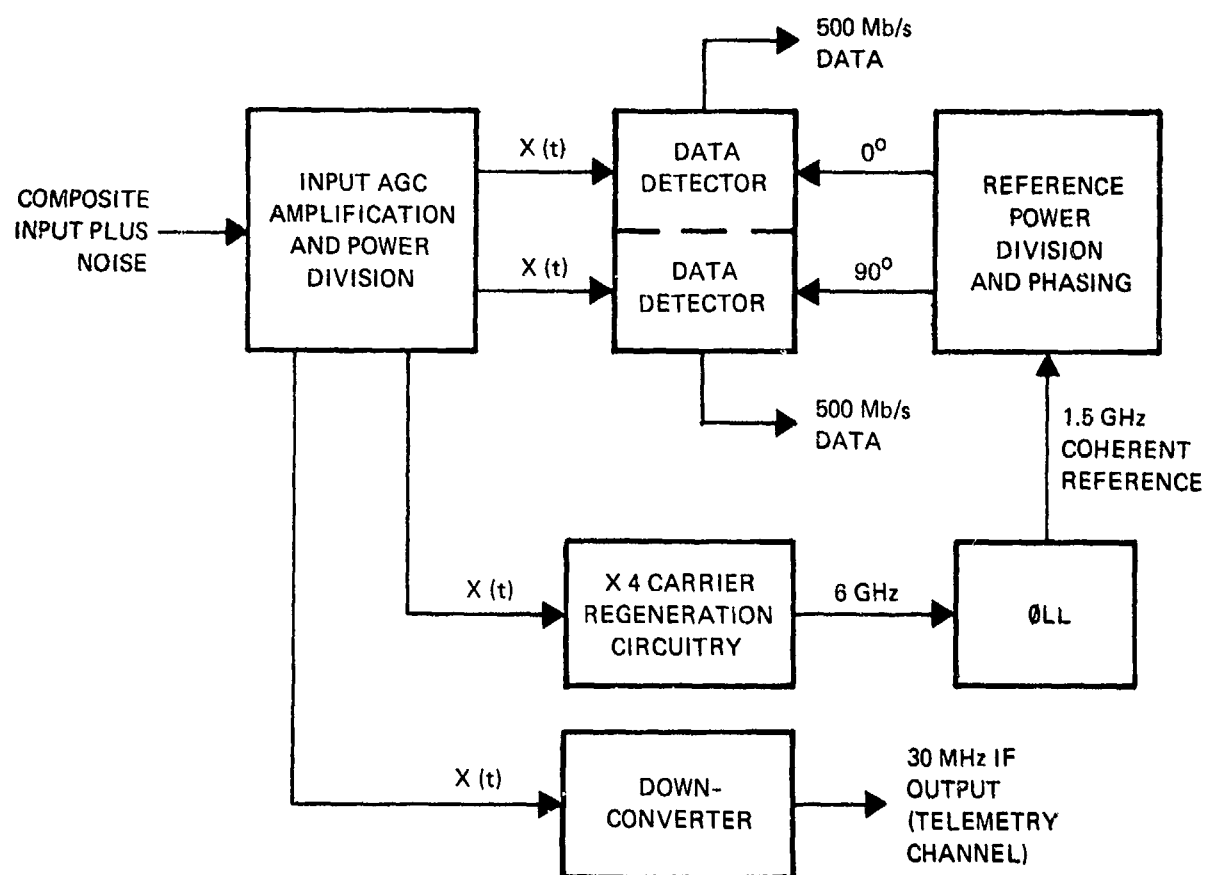
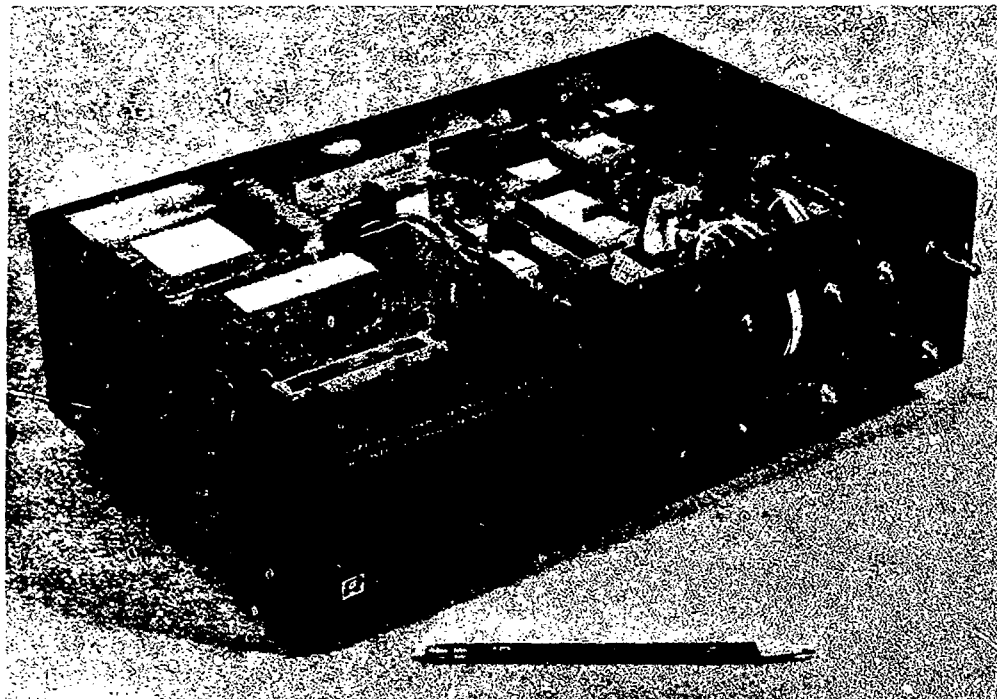
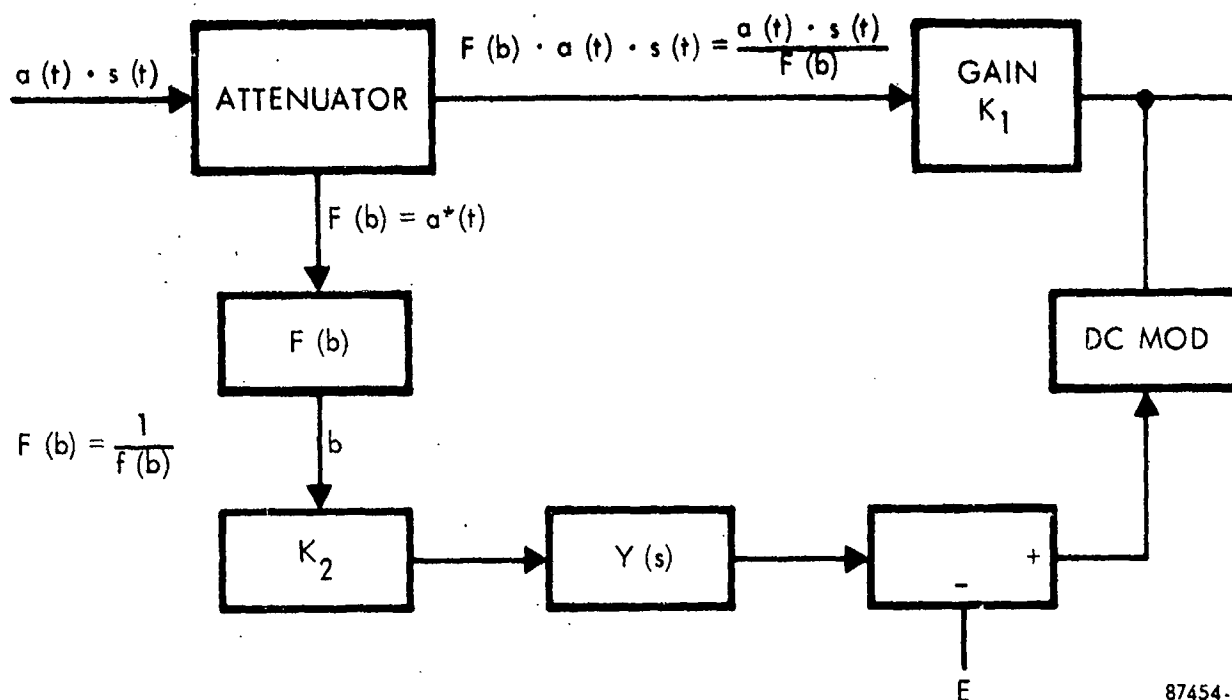
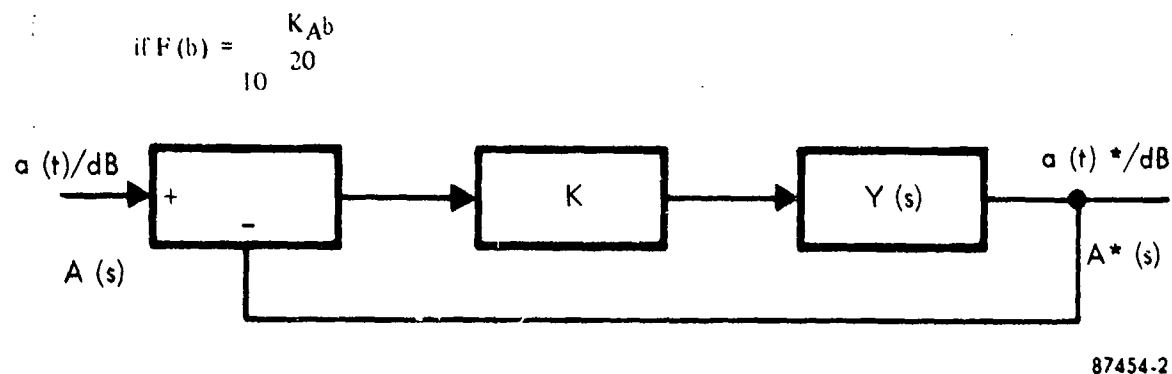


Figure 15. 1 Gb/s QPSK Demodulator Plus 100 kb/s PSK Downconverter



The loop can be analyzed by introducing the envelope concept. The input is considered to be at  $a(t) \cdot s(t)$  where  $a(t)$  is a positive real function that varies slowly compared to  $s(t)$  which is a constant amplitude periodic function. This model can then be transformed to the following configuration:



where  $20 \log_{10} a(t) = a(t)/\text{dB}$   
 $20 \log_{10} a^*(t) = a^*(t)/\text{dB}$   
 $A(s) = \text{Laplace transform of } a(t)/\text{dB}$   
 $A^*(s) = \text{Laplace transform of } a^*(t)/\text{dB}$   
 $\frac{A^*(s)}{A(s)} = \frac{K Y(s)}{1 + K Y(s)}$

Thus, there is a linear equivalent loop for the input and output in decibels. For the transfer function  $Y(s)$  a one-pole filter will be used. Thus,

$$\text{if } Y(s) = (K_y) \left( 1 + \frac{1}{R_2 C} s \right)$$

$$\text{then } \frac{A^*(s)}{A(s)} = \frac{K(K_y)}{(K(K_y) + 1) + s R_2 C}$$

The total required gain  $K(K_y)$  can be determined by considering the static gain as follows:

$$\frac{A^*(0)}{A(0)} = \frac{K(K_y)}{K(K_y) + 1}$$

Thus, for the requirement that gain change over the 20 dB dynamic range be less than .5 dB:

$$\frac{A^*(0)}{A(0)} = \frac{K(K_y)}{K(K_y) + 1} = .975$$

$$K(K_y) = 39$$

Then, for

$$K(K_y) = K_A \cdot K_d \cdot K_y = 39$$

$$K_y \approx 150$$

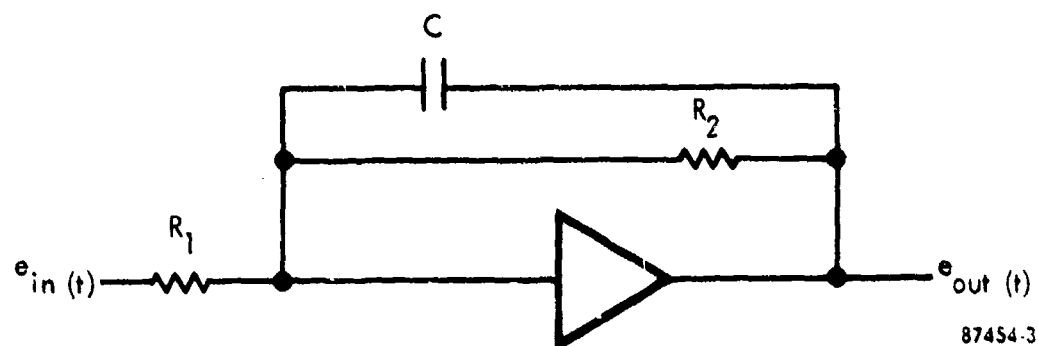
Next to be considered is the bandwidth of the AGC loop. For:

$$\frac{A^*(j\omega)}{A(j\omega)} = \frac{39}{39 + j\omega R_2 C}$$

Then, for a 3 dB bandwidth of 200 Hz

$$R_2 C = \frac{39}{2 \pi \cdot 200 \text{ Hz}}$$

The AGC loop filter is configured as shown and



has a transfer function that can be represented as follows:



$$\frac{E_{out}(s)}{E_{in}(s)} = \frac{-R_2}{R_1} \left[ \frac{1}{1 + R_2 C} \right]$$

Thus, we let

$$Y(s) = \frac{R_2}{R_1} \left[ \frac{1}{1 + R_2 C} \right]$$

and  $(K_y) = \frac{R_2}{R_1}$

Therefore, from the bandwidth and static gain requirements that:

$$f_{(3\text{ dB})} = 200 \text{ Hz}$$

$$K_y = 150$$

$$R_2 C = .031 \text{ second}$$

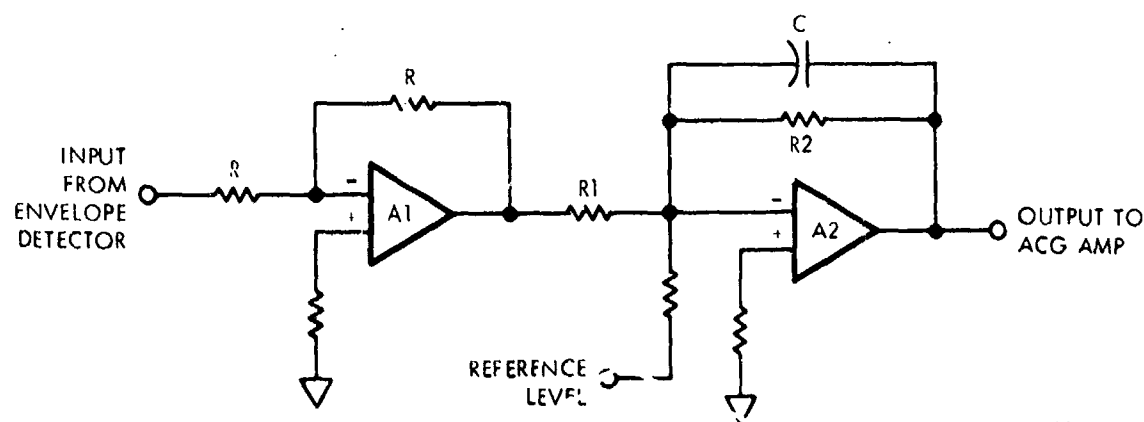
The component values are calculated and presented as follows:

$$C = .05 \mu\text{F}$$

$$R_2 = 620\text{K}$$

$$R_1 = 4.1\text{K}$$

The resulting overall loop filter with an inverting unity gain operational amplifier circuit between the loop filter and the envelope detector is shown in Figure 16. The inverting amplifier buffer stage is required so that the

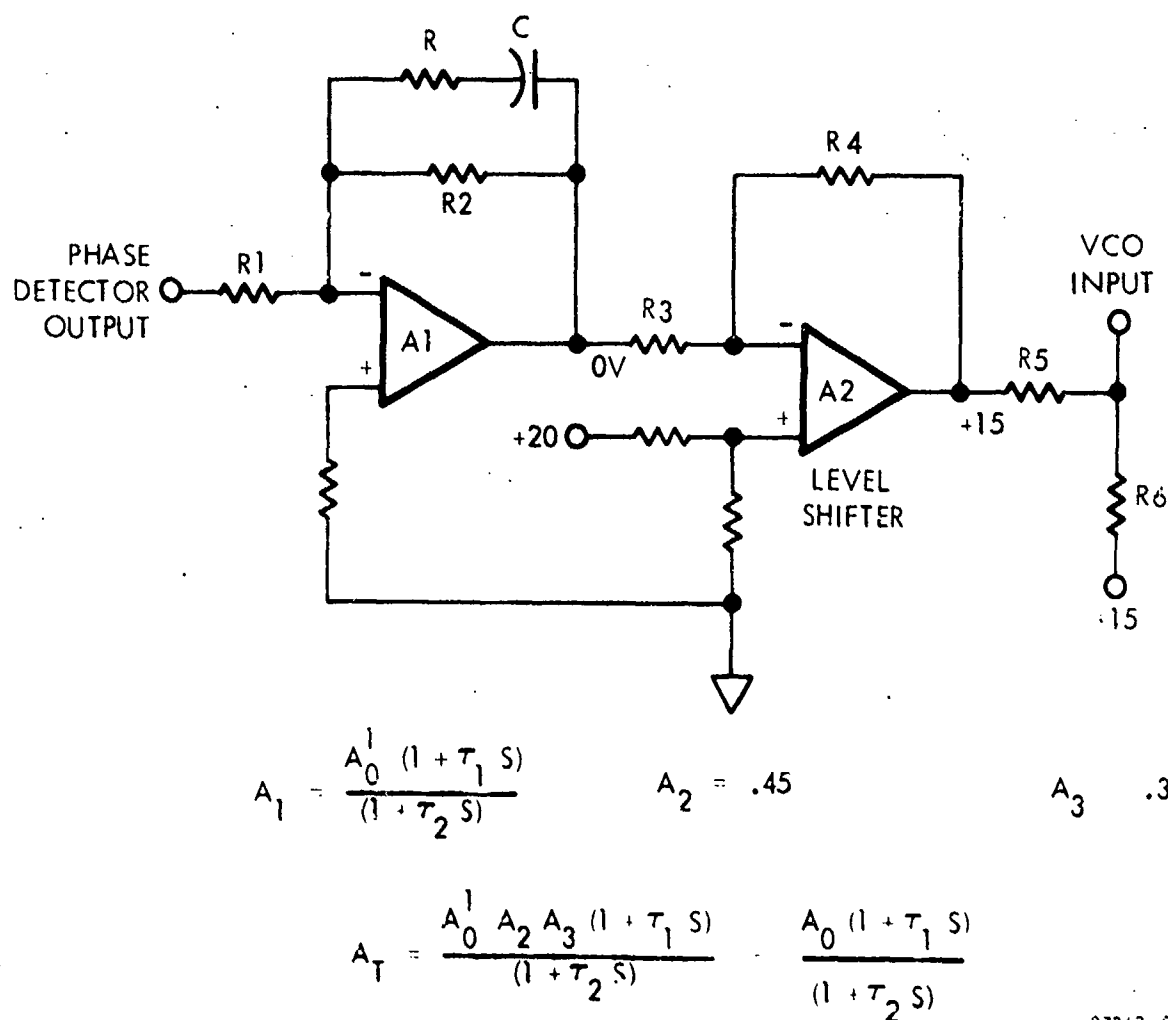


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Figure 16. AGC Loop Filter-Demodulator

feedback would have the proper sign. In the performance tests chapter it will be shown that the BER performance of the QPSK system is essentially constant over a 20 dB range of input power as desired.

The carrier regeneration technique amplifies one of the  $X(t)$  signals, bandpass filters it, and then routes the wideband signal through an X4 nonlinearity to generate an unmodulated carrier reference at 6 GHz. In the phase-lock loop a 6 GHz multiple of the 1.5 GHz VCO is compared in a phase detector to the reference carrier input. The X4 multiple of the VCO is phase locked to the unmodulated 6 GHz reference. The 1.5 GHz VCO frequency then provides the coherent reference for demodulation. Design considerations for the phase-lock loop are now presented. The loop filter has the transfer function,  $A_0 \frac{(1 + \tau_1 s)}{(1 + \tau_2 s)}$ , which results in an overall closed-loop transfer function of the form,  $\frac{1 + as}{1 + bs + cs^2}$  as desired. A simplified schematic of the loop filter is presented in Figure 17.



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Figure 17. Loop Filter for 1 Gb/s QPSK Demodulator Phase-Lock Loop

The first stage implements the desired transfer function. The second stage level shifts the normal zero-volt output of  $A_1$  to the +15 volt level required at the VCO input. A network including  $R_5$  and  $R_6$  is used for filtering and isolation between the VCO input and amplifier  $A_2$ 's output. The rolloff of  $A_2$  is well beyond the unity gain crossover frequency of the loop.

Design parameters for the design equations are:

$$\text{VCO gain } K_O = 10^9 \text{ rad/volt}$$

$$\text{Phase Detector Gain } K_D = 5 \times 10^{-3} \text{ vol./rad}$$

The steady state phase error,  $\phi_{\text{ess}}$ , of the loop for a static frequency offset of the unlocked VCO relative to the reference input is

$$(1) \quad \phi_{\text{ess}} = \frac{\Delta\omega}{1 + K_O \cdot K_D \cdot A_O} \approx \frac{\Delta\omega}{K_O \cdot K_D \cdot A_O}$$

The stability of the transmitter oscillator is 11.25 kHz and the stability of the VCO over the total range of environmental changes is  $\pm 15$  MHz. Therefore, a reasonable number for maximum  $\Delta\omega$  is  $3\pi \times 10^7$ . Constrain  $\phi_{\text{ess}}$  to be 0.1 radian for this extreme condition so BER degradation would only be several tenths of a dB. A curve of BER versus static phase error for QPSK is presented in Figure 18. Substitution of these values in Equation 1 yields  $A_O = 200$ .

Various analyses\* have been done to relate the noise bandwidth of the phase-lock loop in a QPSK demodulator to the statistical performance. All of these analyses make certain simplifying assumptions to make the mathematics tractable but they can be used as design guides. Using the various equations in these papers, one finds that if the noise bandwidth, BL, is less than 1 MHz for this system then the system degradation due to noise induced timing jitter should be less than 0.2 dB. Let BL equal 100 kHz and choose the damping  $\delta$ , of the loop to be 1 as a compromise between noise bandwidth, mean-time-to-unlock, etc. Now  $\omega_n$  is related to BL by Equation (2).

$$(2) \quad \omega_n = \frac{2 \text{ BL}}{\left(\delta + \frac{1}{4\delta}\right)}$$

Substituting into Equation (2) it is found that  $\omega_n = 1.6 \times 10^5$  radians. Now, time constant  $\tau_2$  can be found by Equation (3).

$$(3) \quad \tau_2 = \frac{K_O \cdot K_D \cdot A_O}{\omega_n^2}$$

Substitution in Equation (3) yields  $\tau_2 = 0.039$ . Time constant  $\tau_1$  is calculated using Equation (4).

$$(4) \quad \tau_1 \approx \frac{2\delta}{\omega_n}$$

Substitution in Equation (4) yields  $\tau_1 = 1.2 \times 10^{-5}$ . One may use Equations (5), (6), and (7) to find  $R_1$ ,  $R_2$ , R and C in the loop filter circuit.

$$(5) \quad (R + R_2) C \approx R_2 C = \tau_2 \quad |A_O| \gg 1$$

$$(6) \quad RC = \tau_1$$

$$(7) \quad |A_O| = R_2/R_1$$

\* See References 1, 2, and 3.

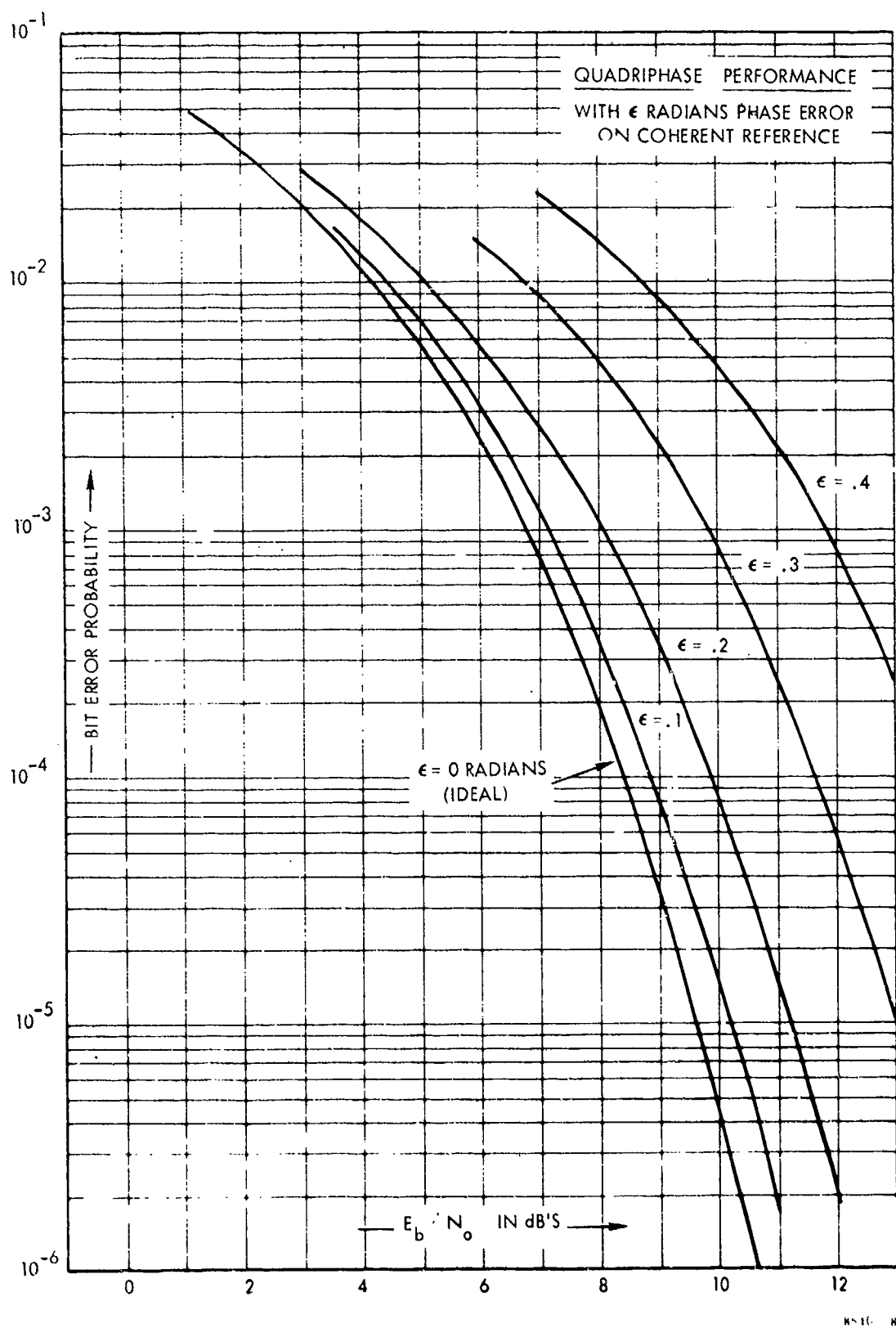


Figure 18. BER Performance as a Function of Static Phase Error

For  $A_0 = 200$  one finds that  $A_0^{-1}$  equals 1500. If  $C = .033 \mu\text{F}$ , a standard value, then one finds with Equation (5) that

$$R_2 = 1.1 \times 10^6 \text{ ohms}$$

since  $|A_0^{-1}| = 1500 = R_2/R_1$ , one now finds that  $R_1 = 730 \text{ ohms}$

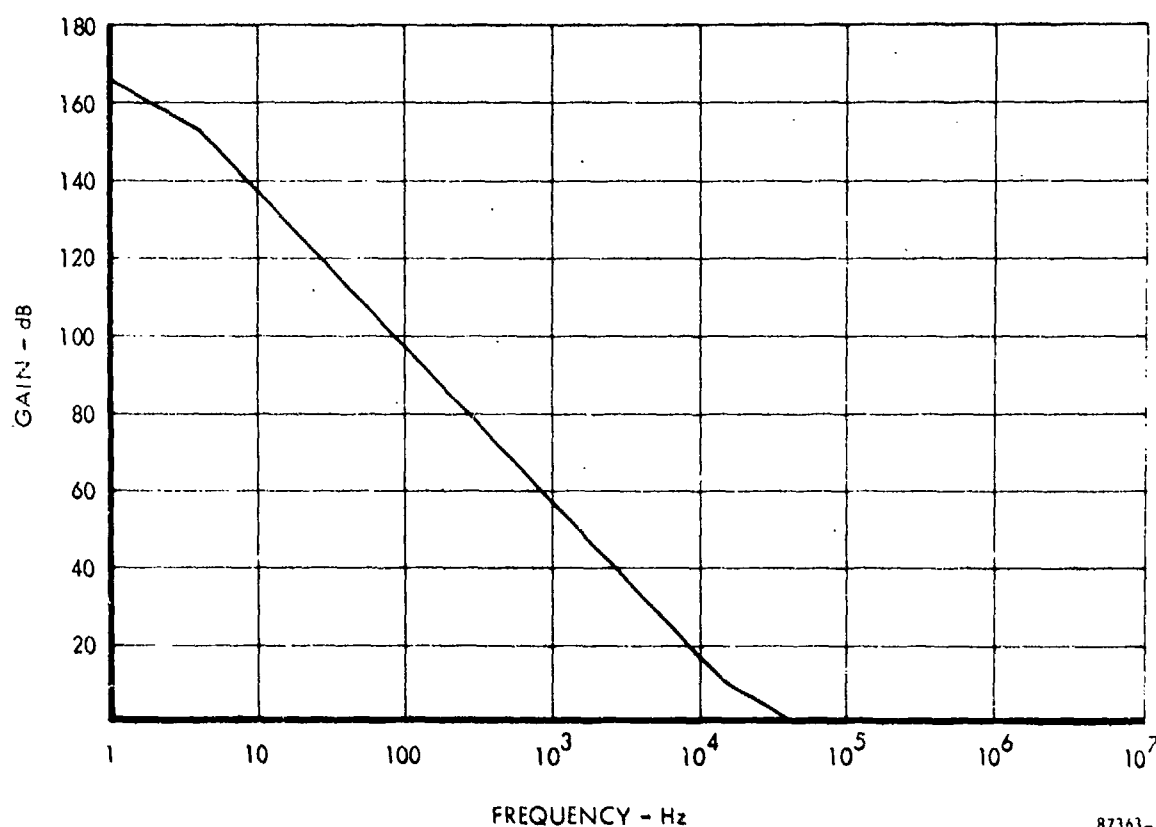
now 
$$R = \frac{\tau_1}{C} \approx 360 \text{ ohms}$$

The unity gain frequency of the open loop phase-lock loop response is found from Equation (8)

$$(8) \quad f_\mu = 2\delta f_n$$

$$\therefore f_\mu = 51 \text{ kHz}$$

A Bode plot of the open loop phase-lock loop response is given in Figure 19. The VCO-multiplier could have been implemented by interconnecting discrete units such as a VCO, power splitter, comb generator, and filters.



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Figure 19. Phase-Lock Loop Open-Loop Response - Demodulator

Such an arrangement would perform properly but it seemed desirable to purchase the VCO-multiplier as one unit from a vendor rather than interconnecting multiple parts. Therefore, Radiation specified the desired unit and received bids on it. At the start of this program two units were ordered from the selected vendor. One was purchased by Radiation for internal use and the other was purchased for the deliverable system. The plan was that the first VCO-multiplier would be Radiation's. It was to be tested and any desired changes would be made in the second unit. The second unit would then be used in the deliverable Air Force system. Due to component delivery problems, the vendor delivered the first unit late enough so that it had to be used in the deliverable demodulator. The second unit was not received until a month after the shipment of the deliverable system. Therefore, we did not have the benefit of testing the first unit before accepting the second unit. The first unit performed adequately but had two characteristics which represented problems. The first was that the dc offset required at the voltage control input was +15 volts, an amount greater than the specification. Therefore, the loop filter board had to be modified so that the second operational amplifier was powered only by a plus supply. This amplifier was used to level shift to the required dc level. The second undesirable characteristic of the VCO-multiplier was the fact that the unit is microphonic. There was not sufficient time to send the unit back to the vendor for modification so we had to live with this problem. This problem was pointed out to the vendor and the second unit does not have this problem.

## Section V

### DESIGN CONSIDERATIONS FOR THE 500 Mb/s BIT SYNCHRONIZER-SIGNAL CONDITIONER (BSSC)

A block diagram and photograph of this unit are repeated in Figure 20. Consider the matched filter-amplification function. The type of matched filter that is approximated is the sliding integral shown in Figure 21. The filter output is always the integral over the last  $T$  seconds where  $T$  is chosen to be a bit period. The impulse response,  $h(t)$ , is rectangular as shown. For over five years Radiation has used various polynomial approximations,  $H^1(s)$  to the sliding integral in its high bit rate BSSC's.\* This technique consists of adjusting, by various analytical and computer techniques, the coefficients of a transfer function,  $H^1(s)$ , so that its impulse response,  $h^1(t)$ , matches  $h(t)$  as optimally as possible. The technique involves first choosing transfer functions  $H^1(s)$ , that have desirable properties; adjusting the coefficients of the polynomials for best fit; and calculating the BER versus SNR performance of the optimized approximation.

The next significant problem is implementation of a given  $H^1(s)$  with a network using real-world components. This usually involves both discrete and distributed networks and is a very difficult problem at high bit rates due to the nonideal nature of components, networks, etc., over such a broad baseband bandwidth. The effect of poles and zeros at several times the bit rate on the statistical performance can be significant.

The particular filter implemented gives a good approximation to the sliding integral response but is adjustable. The adjustment capability was desirable for the following reasons. When used with a QPSK demodulator, the analytic low-pass equivalent of the demodulator bandpass filtering due to amplifiers, filters, etc., is part of the overall baseband filtering. For optimum performance the filter is adjusted so that the combination of the equivalent low-pass demodulator filter and the BSSC filter represents a matched filter. The filter can also be adjusted to compensate, within reasonable limits, for other post-transmission filtering before the demodulator. If there is pre-transmission filtering, the adjustment capability allows one to alter the low-pass filtering impulse response to more closely represent a matched filter for the signal transmitted. Thus, better statistical performance can be obtained.

The rest of the signal conditioner consists of the decision unit and the demultiplexer. The matched filter output,  $y(t)$ , is routed to the decision unit where  $y(t)$  is compared to a reference level  $\epsilon$ . A narrow pulse is generated if  $(y(t) - \epsilon)$  is negative at the end of a given bit period. If  $(y(t) - \epsilon) > 0$  at the end of the bit period, no pulse is generated. These pulses are the input to logic circuitry that generate a 500 Mb/s data estimate bit stream. The timing of the decision process is controlled by the bit rate clock output of the bit synchronizer. The 500 Mb/s data estimate output is also demultiplexed into two output 250 Mb/s data streams at MECL III levels for convenience in testing. The bit rate clock divided by two controls the demultiplexer and is also provided as an output.

The bottom half of Figure 20 is the bit synchronizer. The bit synchronizer posed some unique problems that required the use of a sweep circuit in the phase-lock loop. This was due to the  $\pm 1\%$  or 10 MHz variance in bit rate specification. A more detailed block diagram of the bit synchronizer is presented in Figure 22. After  $y(t)$  is full-wave rectified, the resulting bit rate spectral component is bandpass filtered to enhance signal-to-noise ratio and to provide memory for no transitions. To handle a 10 MHz range the bandpass filter must have at least this bandwidth. Since phase shift through the filter directly affects the time at which bit decisions are made, the bandwidth was chosen as 25 MHz to minimize the variation in phase shift with bit rate. With such a wide bandwidth, the SNR improvement and memory are less than desirable. To minimize timing jitter, the phase-lock loop noise bandwidth must be greatly reduced to achieve BER performance close to theoretical. The narrow loop, however, must lock over a 10 MHz range which is greater than the acquisition range of such a loop. This problem was solved by adding a free-running sweep input to the VCO so that the VCO frequency sweeps over the range of bit rates. This lockup is assured if the sweep rate is less than the  $\omega_n$  of the loop squared. The loop filter gain was chosen so that in a phase locked condition the time varying phase error due to the sweep input is less than two degrees total.

\* See References 4, 5, and 6.

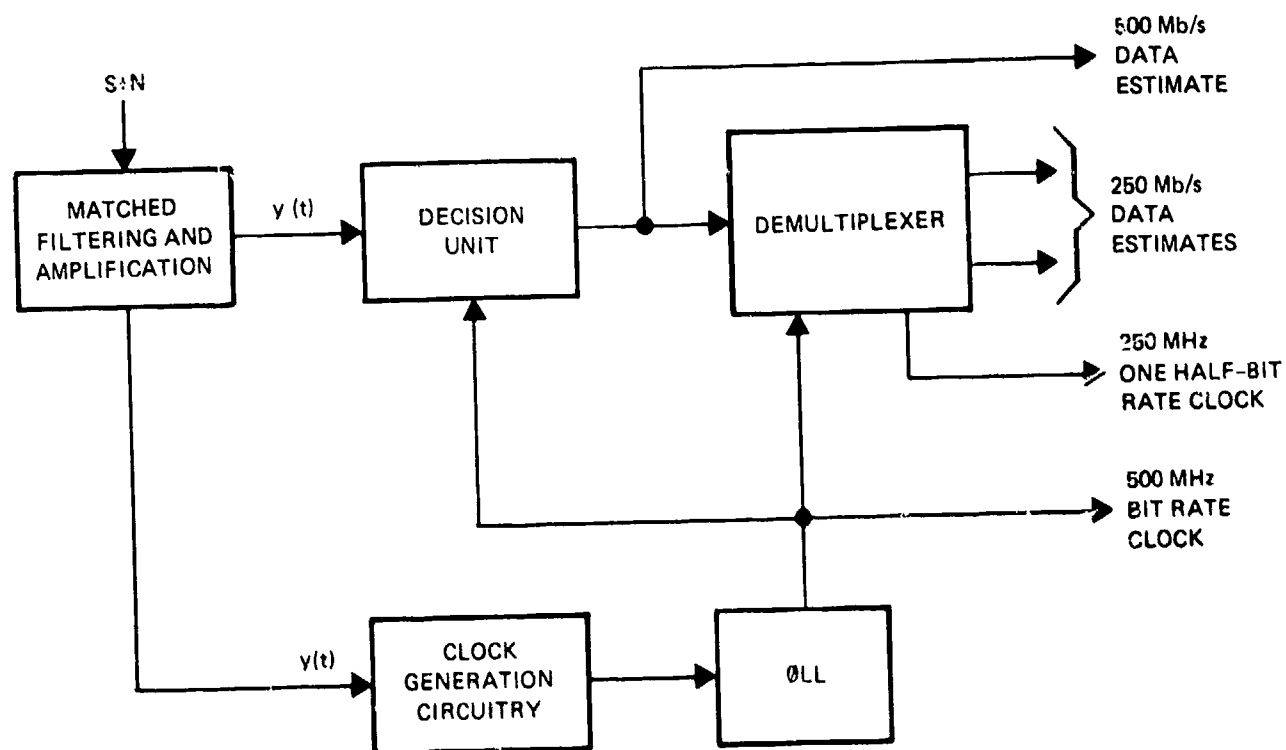
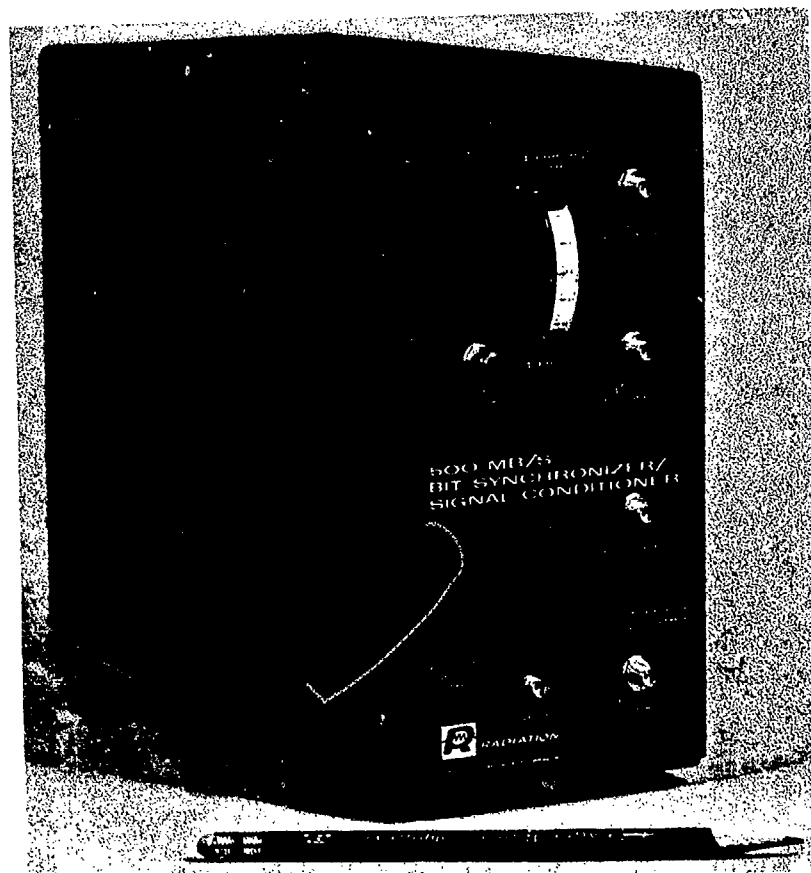
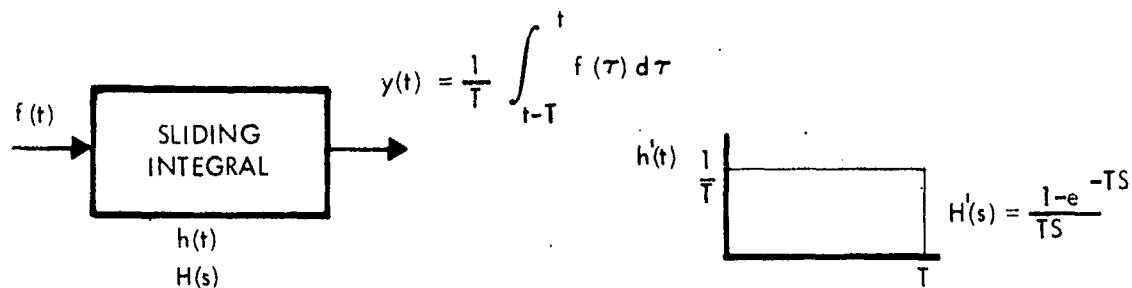
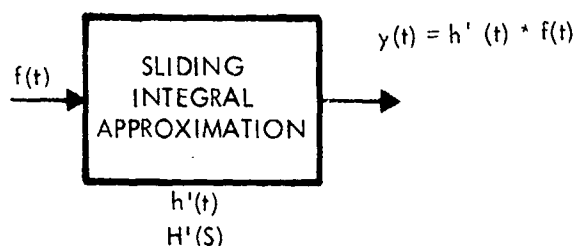


Figure 20. 500 Mb/s Bit Synchronizer-Signal Conditioner (BSSC)

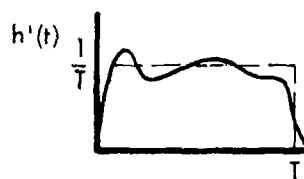




#### APPROXIMATION



#### AN EXAMPLE APPROXIMATION



POLYNOMIAL APPROXIMATION

$$H'(s) = \frac{a_N s^N + a_{N-1} s^{N-1} + \dots + a_1 s + a_0}{b_N s^N + b_{N-1} s^{N-1} + \dots + b_1 s + b_0}$$

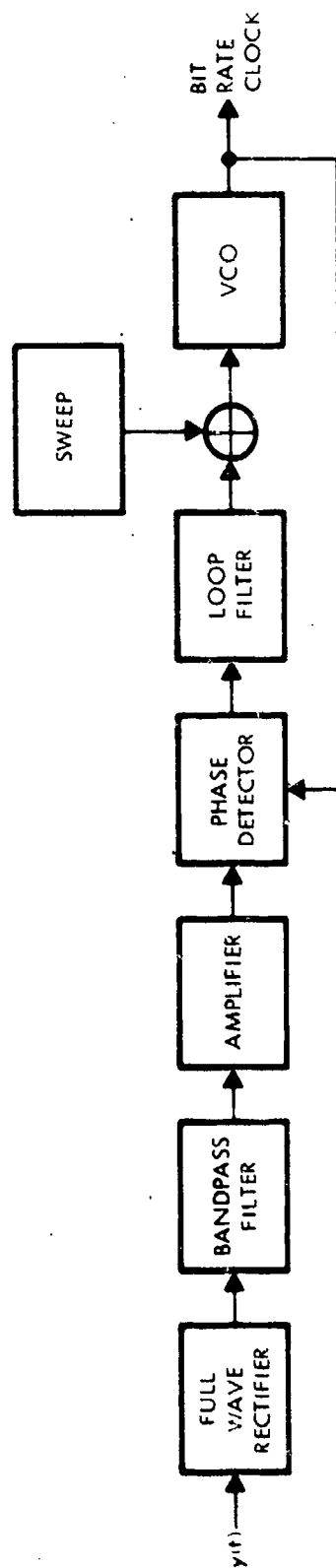
87363-6

Figure 21. Sliding Integral Matched Filter and Approximation

It was calculated that the effect on BER should be negligible and this was experimentally verified. Therefore, the sweep could be made free running and circuitry to detect lock and to disable the sweep could be eliminated.

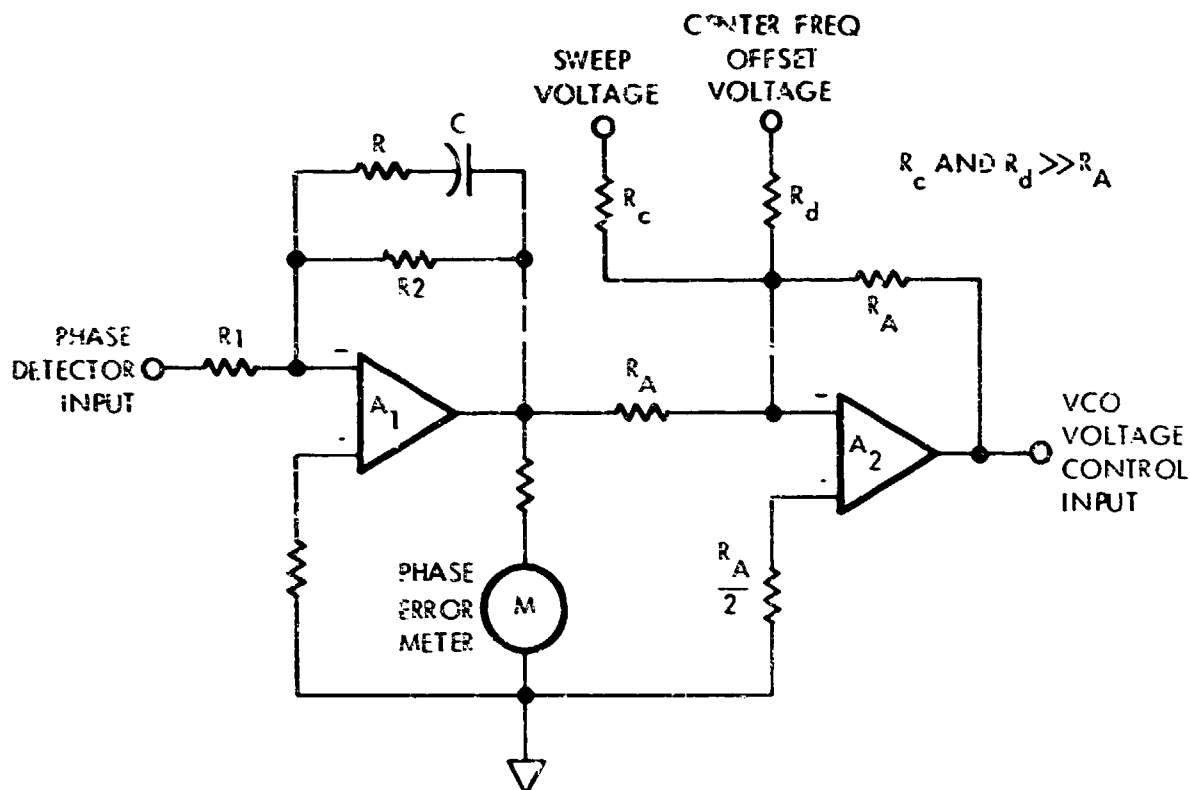
Standard product 500 MHz VCO's having desirable properties delivered an output power of approximately 150 milliwatts. Only 30 to 40 milliwatts were required and a higher speed than normal voltage control input was desirable. At the start of this program Radiation negotiated a nonstandard VCO specification with the selected vendor and these units were procured for this program. These units consumed only .45 watt of the dc power compared with 2.4 watts for the standard VCO. The voltage control input frequency response was measured on all units using the Bessel null technique and was found to be essentially flat to 3.5 MHz. Measurements above 3.5 MHz could not be made without over deviating the VCO frequency. Such response ensures that natural frequencies due to the VCO are well outside the phase-lock loop frequency region of gains greater than unity. This helps to ensure stability and actual response close to that calculated.

The phase-lock loop filter design is now presented. In Figure 23 a simplified schematic of the loop filter is presented. The transfer function of the filter is  $\frac{A_0(1 + \tau_1 s)}{(1 + \tau_2 s)}$  so that the overall phase-lock loop transfer function is  $\frac{1 + as}{1 + bs + cs^2}$  as desired. In the schematic it is seen that operational amplifier A1 is used to implement the desired



87363-5

Figure 22. Bit Synchronizer of BSSC



$$A_{1V} = \frac{-A_o (1 + \tau_1 s)}{(1 + \tau_2 s)}$$

$$A_{2V} = -1$$

87363-4

Figure 23. Simplified Schematic for Bit Synchronizer Phase-Lock Loop Filter

filter transfer function. Its output drives the phase error meter and the VCO through A2. Amplifier A2 transmits A1's output to the VCO input with a gain of -1. The output of A2 is also dc offset to provide the proper center frequency and has the sweep voltage summed with other outputs. Parameters for the design equations are:

VCO gain  $K_o = 3 \times 10^8$  radians/volt

Phase detector gain:  $K_D = 5 \times 10^{-2}$  volts/radian.

To achieve performance close to theoretical for such a wide bandwidth bandpass filter preceding the phase-lock loop,  $\phi_{LL}$ , the  $f_N$  of the  $\phi_{LL}$  is chosen to be .003% of bit rate or  $f_N = 15$  kHz. The steady-state phase error,  $\phi_{ess}$ , of the loop for a static frequency offset of the unlocked VCO relative to the bit rate input is

$$(1) \quad \phi_{ess} = \frac{\Delta\omega}{1 + K_o K_d A_o} \approx \frac{\Delta\omega}{K_o K_d A_o} \quad K_o K_d A_o \gg 1$$

A reasonable number for  $\phi_{ess}$  based on BER degradation is  $\phi_{ess} = 1^\circ$  for  $\Delta\omega = 1\% \omega_{BR}$ .  $\therefore \Delta\omega = \pi \cdot 10^7$  and  $\phi_{ess} = \frac{\pi}{180}$ . Substitution in Equation (1) yields that  $A_o$ , the dc gain of the loop filter, should be 115.

Time constant  $\tau_2$  is found by Equation (2)

$$(2) \quad \tau_2 = \frac{K_O \cdot K_d \cdot A_O}{\omega_n^2}$$

Substitution in Equation (2) yields  $\tau_2 = .83$ .

Time constant  $\tau_1$  is calculated by the use of Equation (3)

$$(3) \quad \tau_1 \approx \frac{2\delta}{\omega_n}$$

The  $\delta$  of the loop is chosen to be 1 as a compromise between noise bandwidth, mean-time-to-unlock, etc.

$$\therefore \tau_1 = 2.12 \times 10^{-5}$$

For  $A_O = 115$  one may use Equations (4) and (5),

$$(4) \quad (R + R_2)C \approx R_2 C = \tau_2$$

$$(5) \quad RC = \tau_1$$

to find  $R_1$ ,  $R_2$ ,  $C$ , and  $R$ .

Set  $C = 1 \mu\text{F}$  a standard value

$$\text{then} \quad R_2 = 192 \text{ k}\Omega$$

$$\text{since the } |A_O| = \frac{R_2}{R_1} = 115, \text{ then } R_1 = 1.67 \text{ k}\Omega$$

$$\text{now} \quad R = \frac{\tau_1}{C} = 21.2 \Omega$$

The unity gain frequency of the overall phase-lock loop open-loop transfer function,  $\left[ \frac{K_O \cdot K_d \cdot A_O (1 + \tau_1 S)}{S (1 + \tau_2 S)} \right]$  is

$$f_\mu = \frac{1}{2\pi} \cdot \frac{K_O \cdot K_d \cdot A_O \cdot \tau_1}{\tau_2}$$

$$\text{or} \quad f_\mu = 2\delta f_n$$

$$\therefore f_\mu = 30 \text{ kHz}$$

Resistor  $R_A$  is chosen to be  $2 \text{ k}\Omega$  and the closed-loop pole frequency for amplifier A2 is approximately 6 MHz. Thus, A2 should have no effect on the phase-lock loop response. A Bode plot of the open-loop response of the phase-lock loop is presented in Figure 24.

In conclusion, excellent BER versus SNR performance was achieved for the deliverable BSSC's as shown in Chapter VI. The units occupy a volume small compared to standard rack-mounted BSSC's and operation in the total system is essentially "hands off." The adjustable matched filter capability proved very effective in minimizing overall system BER.

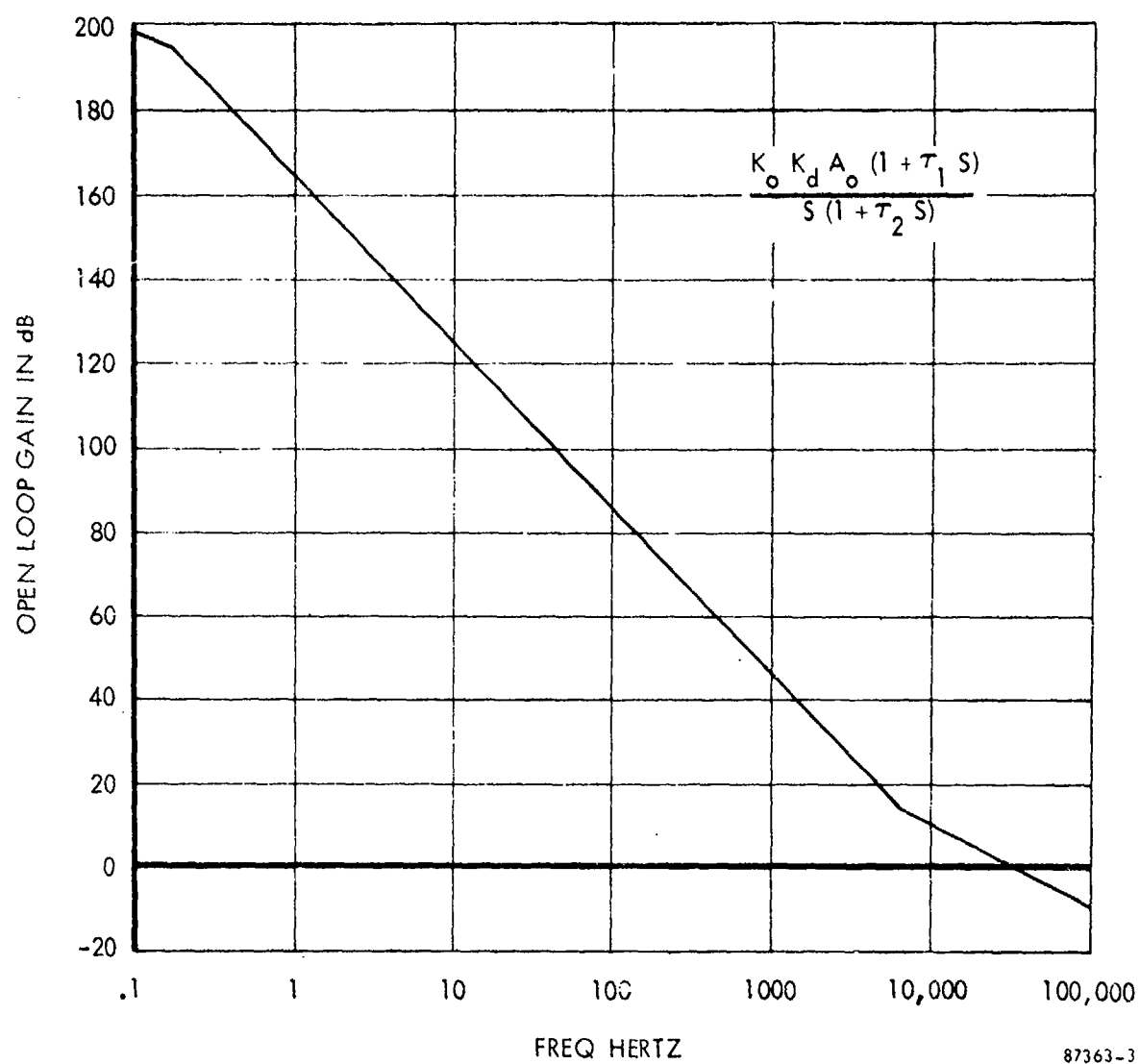


Figure 24. Open-Loop Phase-Lock Loop Response - BSSC

## Section VI

### SYSTEM PERFORMANCE

The measured performance of the deliverable system is now discussed. Bit error rates (BER) were measured over the  $10^{-2}$  to  $10^{-9}$  range. Errors are measured down to such low error rates because the statistical performance of PCM hardware deviates from theoretical at high SNR's, i.e., low error rates. From the user's viewpoint, however, this is the most important region since BER's less than  $10^{-5}$  are usually required. Performance comparisons to that theoretically possible are always with respect to the nonbandlimited PSK theoretical curve. This is mentioned because curves on high data rate systems presented by others have used theoretical performance curves that include various imperfections and make the measured performance appear closer to theoretical.

#### 1. 500 Mb/s BIT SYNCHRONIZER-SIGNAL CONDITIONER PERFORMANCE

In Figure 25 the measured performance of one of the deliverable 500 Mb/s BSSC's is presented. The performance for both units is essentially identical and is within 1.1 dB of theoretical for error rates to  $10^{-9}$ . As mentioned, such performance close to theoretical at high SNR's is quite significant in that all BSSC's diverge from theoretical at high SNR's or low error rates.

The bit slippage rate of the two Air Force BSSC's was also measured. For all units it was better than one part in  $10^9$  bits down to 0 dB  $E_b/N_0$ . One part in  $10^9$  was the limit of the measurement hardware.

#### 2. COMBINED QPSK MODEM-BSSC PERFORMANCE AT 1 Gb/s

The combined modem-BSSC performance at 1 Gb/s for synchronous operation is presented in Figure 26. The measured data is the average of the performance on both output channels for all four possible demodulator lockup positions. The performance is about 1.25 dB from theoretical at  $10^{-6}$  BER and about 1.7 dB from theoretical at  $10^{-9}$  BER. Such performance has been achieved consistently over many tests at different times and locations. To the author's knowledge, such performance equals or exceeds that achieved with QPSK hardware at any bit rate.

#### 3. COMBINED MODEM-BSSC PERFORMANCE OVER AUTOMATIC GAIN CONTROL (AGC) RANGE

The demodulator accepts and automatically gain controls input signals varying from -17 dBm to -37 dBm. The effect of the demodulator AGC over its 20 dB range on the communications performance is illustrated by the three combined modem-BSSC performance curves in Figure 27 for three different levels of input signal power into the demodulator. Within measurement accuracy, all the measured curves are essentially the same and identical to the curve in Section 2. Therefore, the performance comments made in Section 2 hold over the AGC range.

#### 4. ASYNCHRONOUS COMBINED MODEM-BSSC PERFORMANCE

All of the previous curves have been for synchronous operation; that is, the two 500 Mb/s input data streams at the input of the QPSK modulator have had phase coherent bit rates. The effect of asynchronous operation is illustrated by Figure 28. The synchronous operating point shown is at a BER of  $10^{-6}$ . Performance is about 1.25 dB from theoretical. At this SNR the modulator inputs are switched from the synchronous to asynchronous with the difference in bit rates small; the typical case for asynchronous operation. This causes only about 0.2 dB additional degradation in overall performance. As one bit rate is varied above and below the other fixed 500 Mb/s input, the additional degradation in performance is measured. Over a  $\pm 0.6\%$  variation in bit rate, the asynchronous operation is within 0.4 dB of synchronous operation. It should be noted that this testing is done without adjusting either BSSC and for all possible demodulator lockup states. This is considered quite good performance as a  $\pm 0.6\%$  variation in bit rate is quite large for a single-frequency BSSC. The major performance loss mechanism is phase shift through the bit synchronizer bandpass filter in the BSSC that is receiving the bit rate different from 500 Mb/s (see Figure 22). Two methods could be used to minimize this particular loss mechanism. One would be

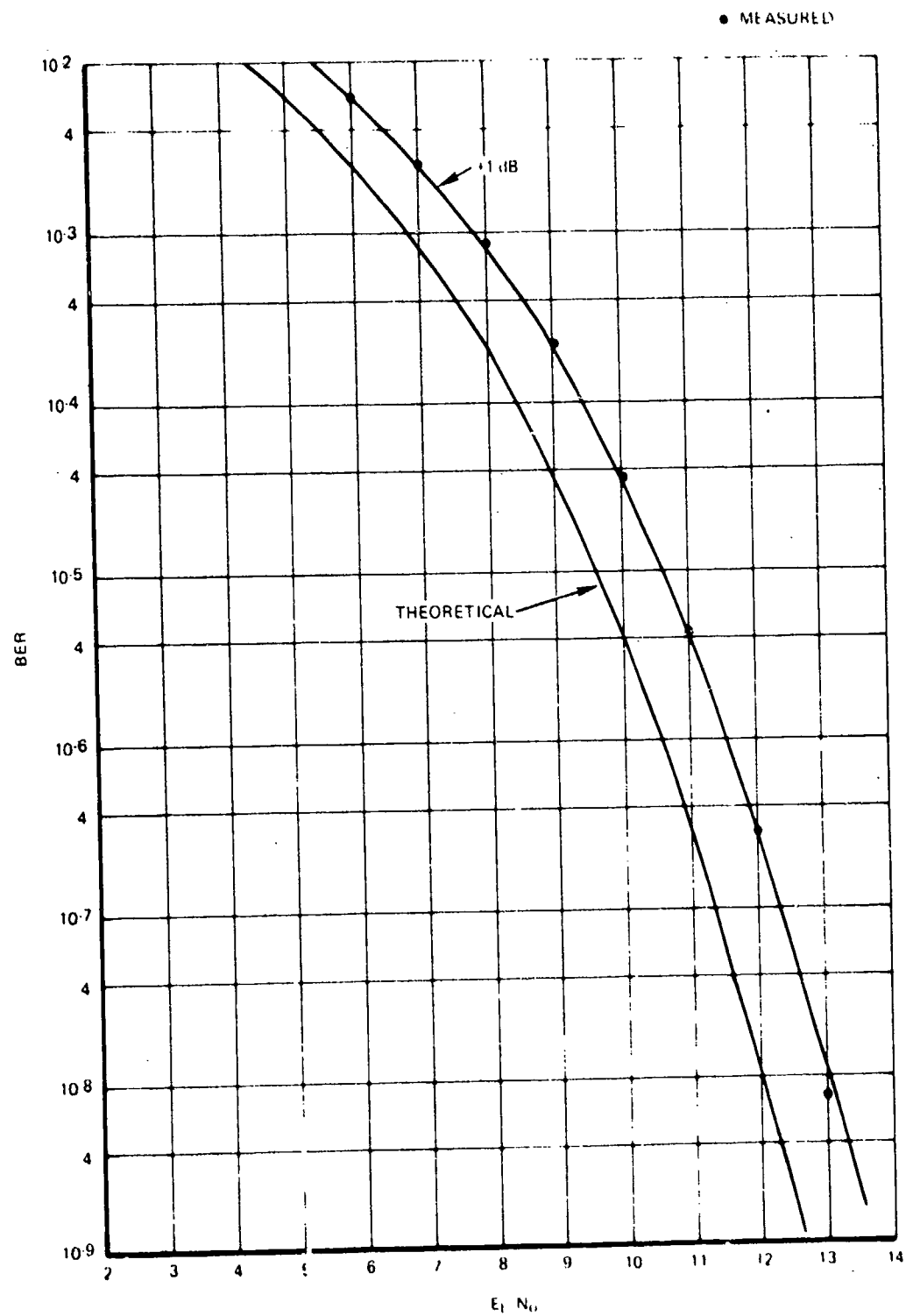


Figure 25. 500 Mb/s BSSC Performance

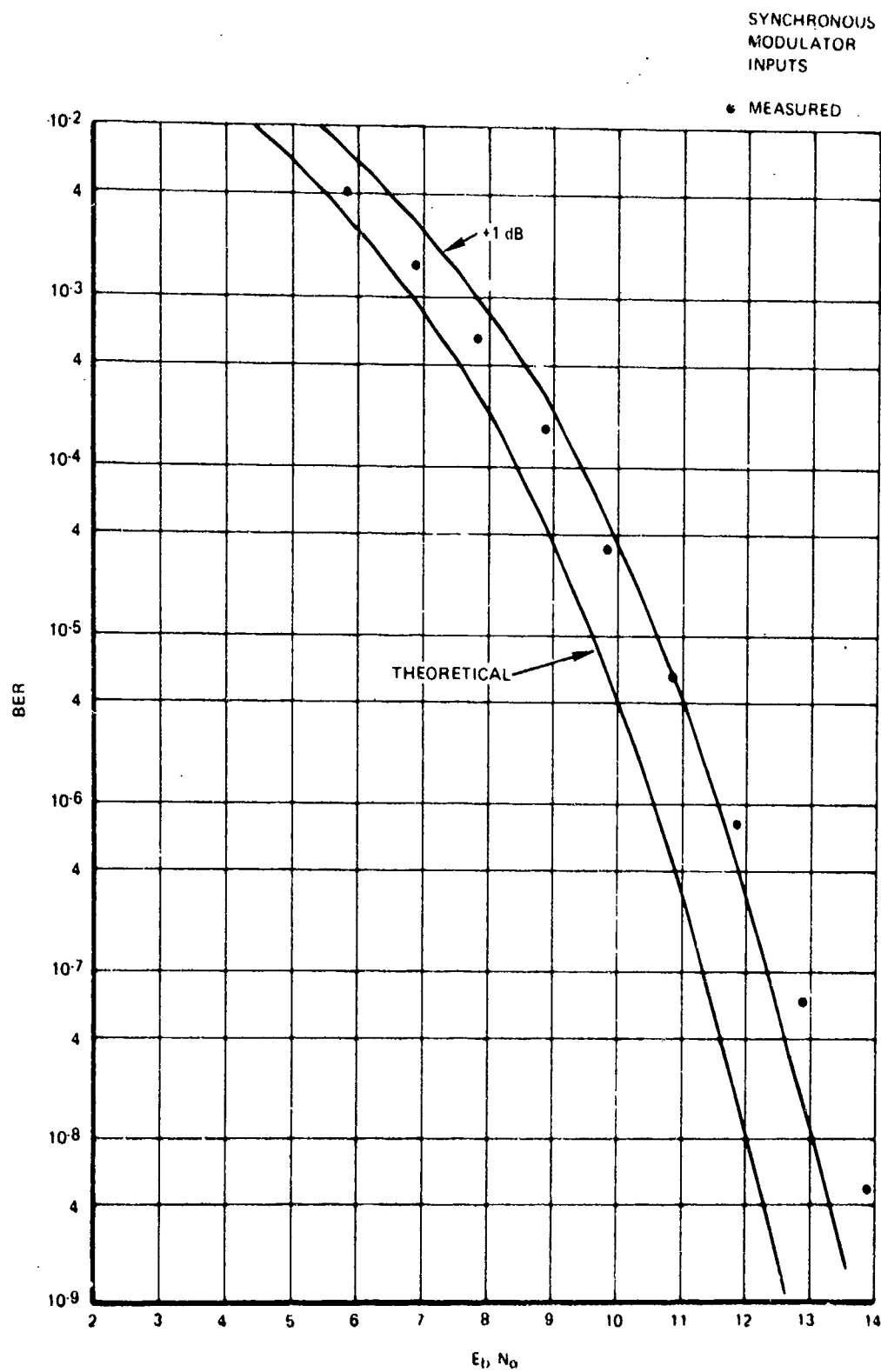


Figure 26. Combined QPSK Modem - BSSC Performance at 1 Gb/s



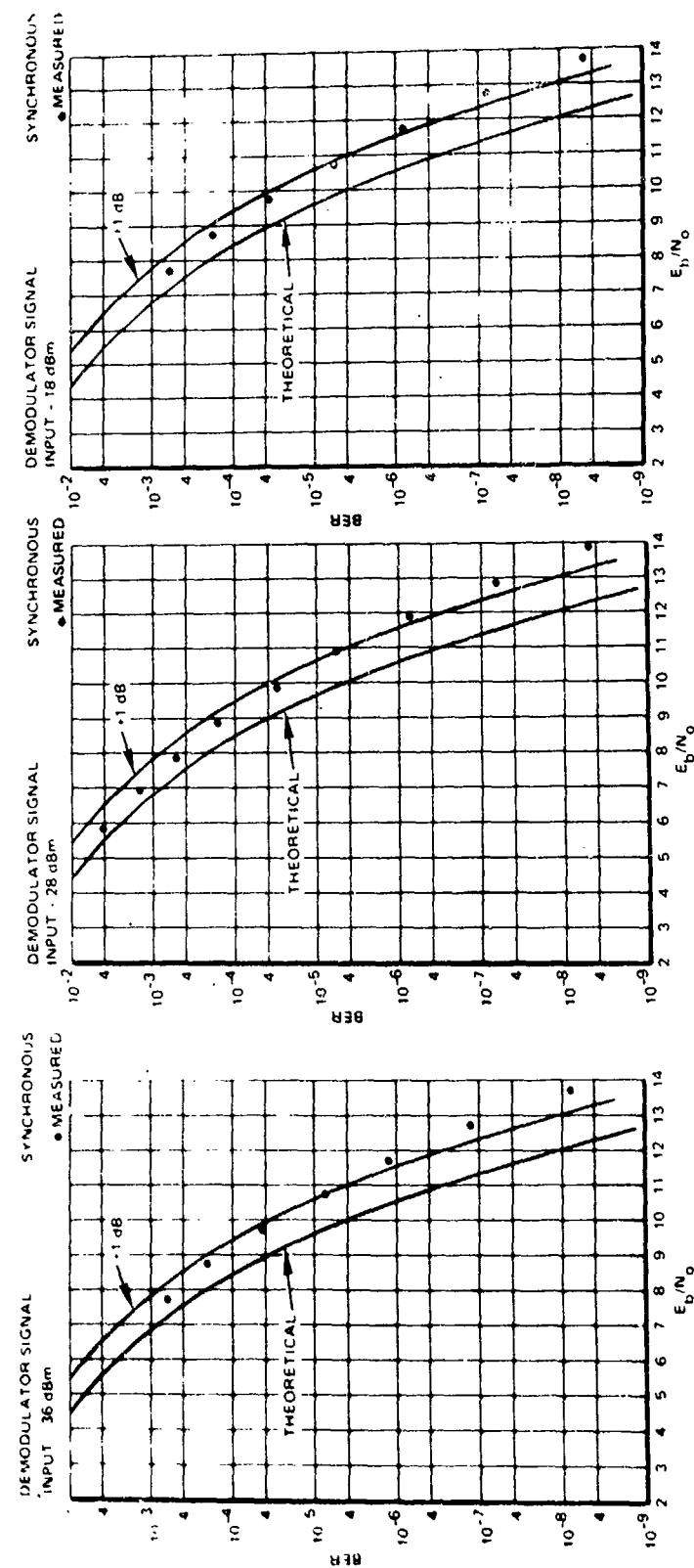


Figure 27. Combined Modem - BSSC Performance Over AGC Dynamic Range

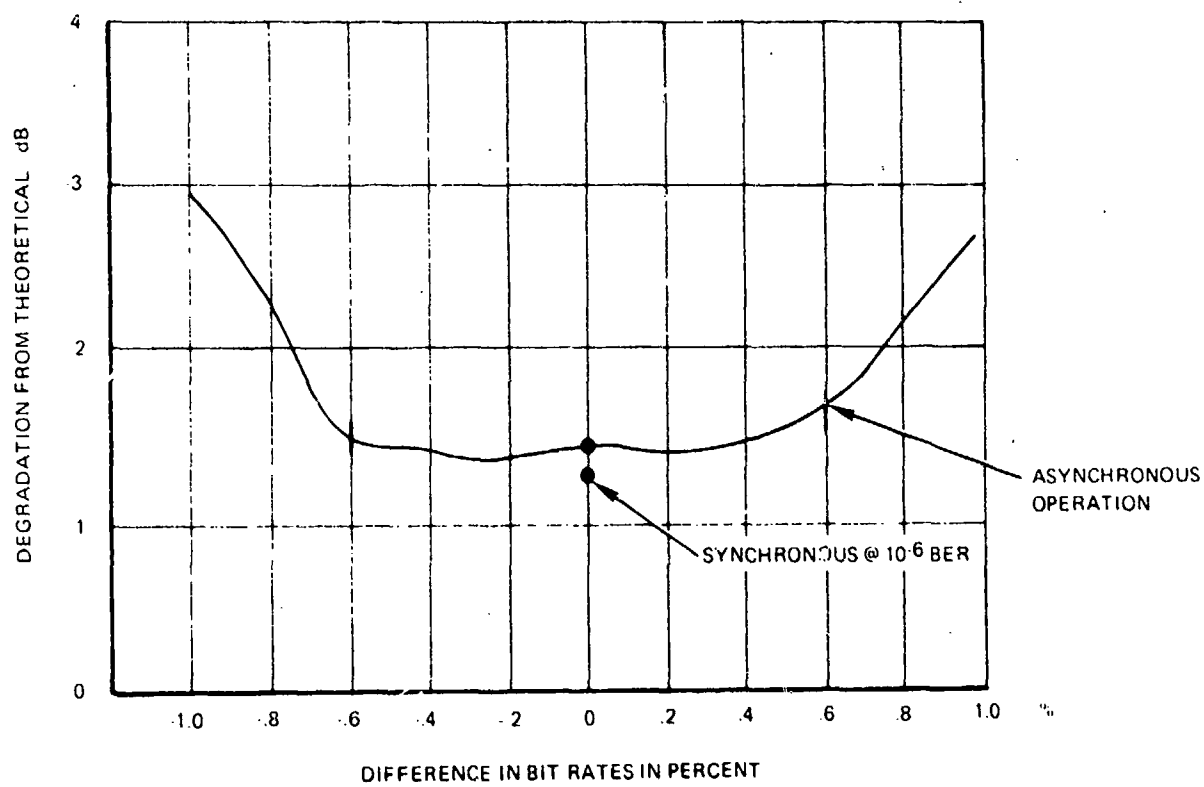


Figure 28. Asynchronous Versus Synchronous Performance

to make the bandpass filter a tracking filter. A much simpler approach that was recently conceived is illustrated in Figure 29. One merely puts an identical bandpass filter between the VCO and the phase detector input. As shown, the VCO phase is now independent of  $\phi$ ; the phase shift through the bandpass filter, when through  $\phi$ , varies with bit rate.

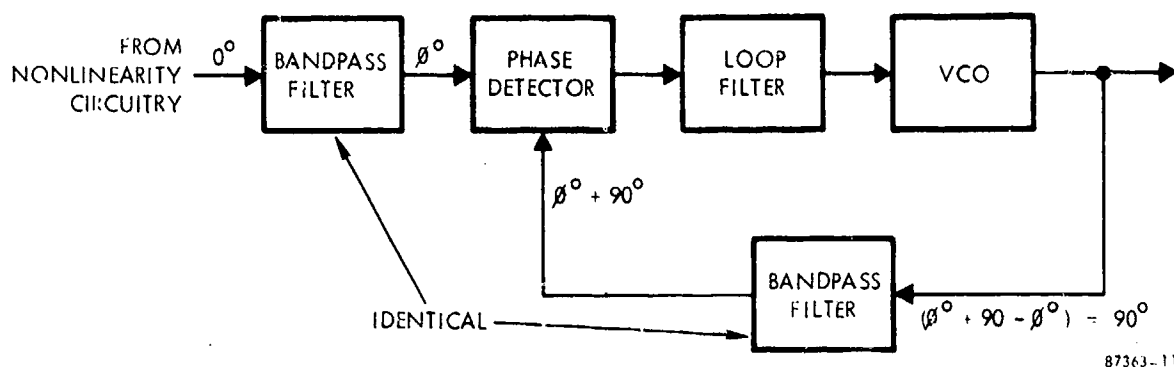


Figure 29. Approach to improve Bit Synchronizer for Varying Bit Rates

## 5. PRETRANSMISSION FILTERING

Due to limitations on the transmitter bandwidth, there may be pretransmission filtering in a 1 Gb/s digital communication system. With the adjustment capability of the BSSC matched filter, one can compensate to better match the transmitted signal and thus optimize system BER performance. This is illustrated in Figure 30 where the 1 Gb/s QPSK modulator is pretransmission bandlimited in a 1 GHz bandpass filter centered at 1.5 GHz. The measured modem-BSSC performance with the BSSC filters adjusted for optimum performance in this condition is presented. It is seen that the performance is as good or better than obtained in the nonbandlimited condition.

## 6. EFFECT OF 100 kb/s TELEMETRY SIGNAL

In all the previous figures representing various conditions, the measured performance is the same for the 100 kb/s PSK telemetry signal on or off. One can detect a very slight increase in error count at any given SNR when the telemetry signal is switched on but the movement in dB from theoretical is indiscernible. Thus, the narrow band signal can be considered to have a negligible effect on the wideband system performance. The legitimate converse question is whether the SNR on the narrow band demodulator output is adequate for low error rate performance of the telemetry channel. In Figure 31 the measured SNR on the demodulator downconverter IF telemetry output is plotted versus the measured wideband SNR at the demodulator input. For this test the wideband signal is on and treated as noise in SNR measurements on the downconverted telemetry IF output. It is seen that the SNR in the telemetry IF is very high. Thus, demodulation and bit estimation of the narrow band telemetry can be accomplished at extremely low error rates, a desirable condition for such telemetry or housekeeping information.

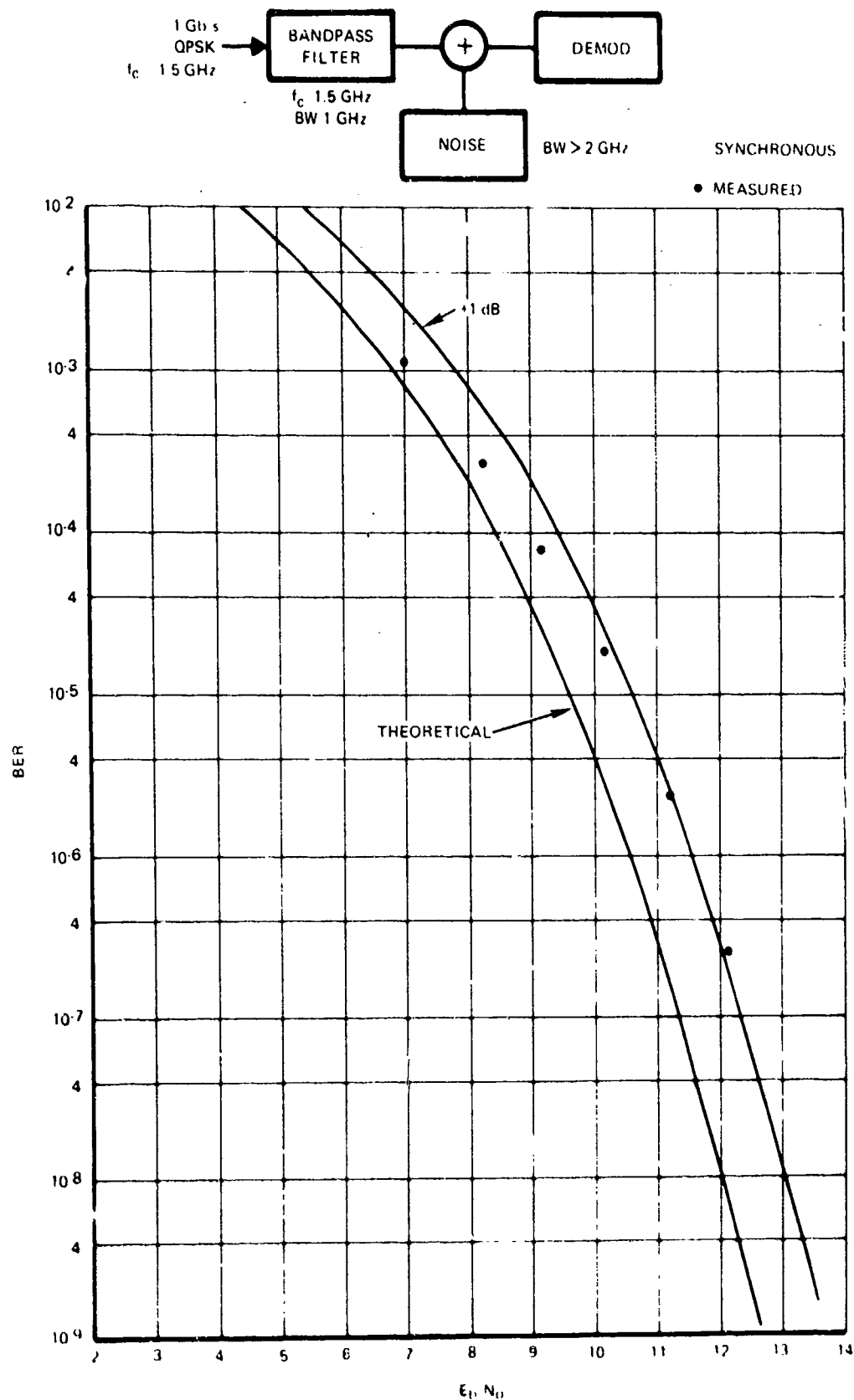


Figure 30. Combined Modem - BSSC Performance at 1 Gb/s For Pretransmission Signal Filtering

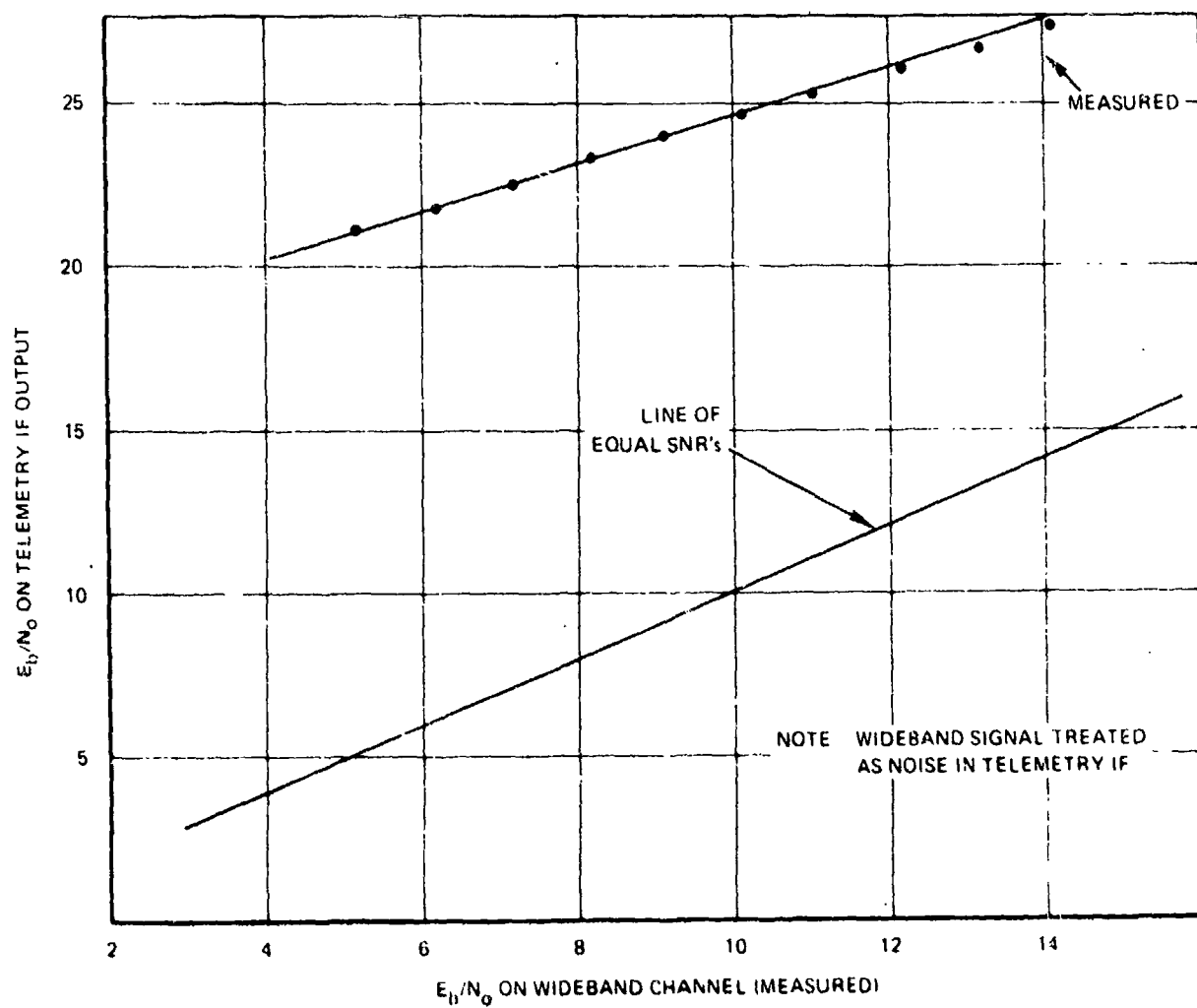


Figure 31. SNR on Telemetry Channel Downconverter Output Versus Demodulator Wideband SNR

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13. ABSTRACT  A Laser Transceiver Electronics system was developed for use in an Air Force Program 405B brassboard 1 Gb/s laser communication system using quadrature phase shift key modulation on a single-frequency laser. This system contains a data source system, BER measurement system, 1 Gb/s QPSK modulator plus 100 kb/s PSK modulator, 1 Gb/s QPSK demodulator plus 100 kb/s PSK downconverter, and two each 500 Mb/s bit synchronizer-signal conditioners (BSSC). Synchronous combined modem-BSSC performance at 1 Gb/s is within 1.3 dB of the nonbandlimited PSK theoretical curve for BER's to $10^{-6}$ over an automatic gain control range of 20 dB and with the 100 kb/s telemetry present. Nonsynchronous performance for close bit rates is within 0.2 dB of the synchronous curve. $E_b/N_0$ on the downconverted telemetry IF output ranges from 20 to 30 dB for a wideband $E_b/N_0$ range of 2 to 14 dB at the demodulator input. The conclusion is that 1 Gb/s QPSK signal processing has advanced to a state where operational hardware is practical.			

14	KEY WORDS	LINK A		LINK B		LINK C	
		ROLE	WT	ROLE	WT	ROLE	WT
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	Bit Synchronizer-Signal Conditioner						
	High Bit Rate						
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